

**NUMERICAL CONTROL OSCILLATOR, DIGITAL FREQUENCY  
CONVERTER AND RADIO FREQUENCY UNIT**

**PRIORITY**

This application claims priority under 35 U.S.C. § 119 to an application entitled  
 “Numerical Control Oscillator, Digital frequency Converter and Radio Frequency Unit”  
 5 filed in the Japanese Intellectual Property Office on December 11, 2002 and assigned  
 Serial No. 359773/2002, the contents of which are incorporated herein by reference.

**BACKGROUND OF THE INVENTION**

1. Field of the Invention

The present invention relates to a numerical control oscillator for  
 10 frequency-converting a received signal into a demodulator input signal through a digital  
 signal process, and a digital frequency converter and radio frequency unit including the  
 same.

2. Description of the Related Art

A conventional numerical control oscillator (NCO) includes a phase data  
 15 accumulator, and a memory (for example, a read only memory (ROM)) for outputting  
 sine data corresponding to a phase calculated by the accumulator. Further, the NCO  
 provides an output frequency defined as follows in Equation (1):

$$F = (F_s \times R) / 2^j \dots (1)$$

where, F is the output frequency, j is a phase word length, F<sub>s</sub> is a sampling  
 20 frequency, and R is an arbitrary integer.

In the case where a target frequency is obtained using a direct digital synthesizer  
 (DDS) that digital/analog-converts and outputs an output signal from the NCO, the  
 output frequency of the NCO can be changed at a 200KHz step by adjusting the  
 sampling frequency of the output signal from the NCO to 200KHz × 2<sup>j</sup> or extending the

phase word length  $j$  (increasing the number of bits) to enhance a phase resolution, or frequency resolution, so that the difference between the target frequency and the output frequency of the NCO is within a range of an allowable deviation.

For example, provided that the sampling frequency  $F_s$  is set to 153.6MHz in a system where the output frequency  $F$  is 1.92GHz and the allowable output frequency deviation  $\Delta f$  is taken at a degree of precision of 0.1ppm, the phase word length  $j$  will be taken as follows in Equation (2):

$$\begin{aligned} j &= \log_2(F_s/\Delta f) \quad \dots (2) \\ &= \log_2(153.6 \times 10^6 / (1.92 \times 10^9 \times 0.1 \times 10^{-6})) \\ &\approx 19.61 \end{aligned}$$

It can be seen from the above Equation (2) that 20 bits are required to define the target phase word length  $j$ .

However, in the case where the phase word length  $j$  is extended, it is necessary to make the phase word length  $j$  equal to a word length  $k$  of the memory (the number of address bits of the memory) ( $j = k$ ) in order to obtain an output signal of the NCO with no spurious effects caused by truncation of phase data. In the case of making the phase word length  $j$  larger than the memory word length  $k$  ( $j > k$ ) in order to suppress an increase in memory size, it is necessary to requantize an address word length (memory word length) output from a phase calculator. This requantization causes the occurrence of an error  $e^p$  of periodicity, which appears as a spurious in the output signal of the NCO (see Henry T Nicholas, III and Henry Samueli, "An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Phase-Accumulator Truncation" in Proc. Annual Frequency Control Symposium, 1987, pp 495-502 (reference 1), for example).

On the other hand, known as a method for suppressing the spurious resulting from the requantization of the address word length from the phase calculator is, for example, a method based on an error feedback or error spread by design (see Jouko Vankka, "Spur. Reduction Techniques in Sine Output Direct Digital Synthesis" in IEEE International Frequency Control Symposium, 1996, pp 951-959 (reference 2), for example). However, as disclosed in reference 1, although the spurious is generated in

the output signal due to the requantization of the address word length from the phase calculator, the phase word length  $j$  inevitably becomes larger than the memory word length  $k$  in order to suppress an increase in memory size.

5 Further, the techniques disclosed in reference 2 are disadvantageous in that additional circuits are required besides the original target circuits, resulting in an increase in circuit size even though the memory size is not increased. The method for suppressing the spurious using the error spread by design involves an increase in noise level (noise floor), so it is not necessarily effective.

10 Moreover, setting the sampling frequency to  $2^j$  times a desired frequency step makes it difficult to generate a reference frequency.

### SUMMARY OF THE INVENTION

Therefore, the present invention has been designed in view of the above and other problems, and it is an object of the present invention to provide a numerical control oscillator for reducing a circuit size and power consumption while maintaining a  
15 desired frequency deviation, and suppressing generation of a spurious effects as much as possible, and a digital frequency converter and radio frequency unit including the same.

In accordance with a first aspect of the present invention, the above and other objects can be accomplished by a numerical control oscillator (NCO) comprising: a phase accumulator for accumulating input phase difference data to generate phase data,  
20 the phase accumulator including a register for storing and outputting the phase data, and a calculator for adding or subtracting the input phase difference data and the phase data from the register to or from each other; and a memory for storing a phase/amplitude conversion table to output amplitude data corresponding to the phase data generated by the phase accumulator, the NCO being adapted to output a signal of a sampling  
25 frequency  $F_s$ , wherein: if an upper limit of a desired frequency setting interval of an output signal is  $FD$  and  $K$  and  $L$  are arbitrary integers, the calculator of the phase accumulator is adapted to add or subtract the input phase difference data and the phase data from the register to or from each other by a modulo operation taking a nearest integer of  $M$  as a modulus, where  $M = F_s/FD \times K/L$ ; and the phase/amplitude conversion

table is adapted to output a signal set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ .

In the NCO with the above-described configuration, if the sampling frequency of the output signal from the NCO is  $F_s$ , the upper limit of the desired frequency setting interval of the output signal is  $FD$  and  $K$  and  $L$  are arbitrary integers, the phase/amplitude conversion table includes  $M$  (integral  $M$ , where  $M = F_s/FD \times K/L$ ) amplitude data, and the phase accumulator generates phase data by accumulatively adding or subtracting the input phase difference data by a modulo operation taking the integral  $M$  as a modulus, and outputs the generated phase data as an address input to the phase/amplitude conversion table. As a result, the phase/amplitude conversion table outputs amplitude data corresponding to the input phase data as an output signal of the NCO set to the frequency setting interval of the  $dF$  step, where  $dF = FD/K \times L$ .

In accordance with a second aspect of the present invention, there is provided a digital down-converter comprising a frequency converter including the NCO of the first aspect as a local oscillator and serving to frequency-convert an input signal sampled at the sampling frequency  $F_s$ , the digital down-converter converting and outputting the input signal into an output signal with a frequency lower than that of the input signal, wherein, if a desired frequency setting interval of the input signal is  $FD$  and  $K$  and  $L$  are arbitrary integers, the frequency converter is adapted to frequency-convert the input signal using a specific signal output from the local oscillator and set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ , the local oscillator outputting the specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M$  as a modulus, where  $M = F_s/FD \times K/L$ .

In the digital down-converter with the above-described configuration, in order to convert and output the input signal sampled at the sampling frequency  $F_s$  into an output signal with a frequency lower than that of the input signal, if the desired frequency setting interval of the input signal is  $FD$  and  $K$  and  $L$  are arbitrary integers, the frequency converter frequency-converts the input signal using a frequency signal output from the NCO of the first aspect as the local oscillator and set to the frequency setting interval of the  $dF$  step, where  $dF = FD/K \times L$ . In the case where the desired frequency setting interval  $FD$  of the input signal is higher than or equal to the frequency setting interval  $dF$  of the frequency converter and is evenly divisible by it, the digital

down-converter can convert the frequency of the input signal input thereto at the frequency setting interval FD into a desired frequency within the range of an allowable frequency deviation.

5 In accordance with a third aspect of the present invention, there is provided a digital down-converter comprising a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert an input signal sampled at a sampling frequency  $F_{s1}$ , and a second frequency converter including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the digital  
10 down-converter converting and outputting the input signal into an output signal with a frequency lower than that of the input signal by two frequency conversions, wherein: if a desired frequency setting interval of the input signal is FD and  $K_1$ ,  $K_2$  and  $L_1$  are arbitrary integers, the first frequency converter is adapted to frequency-convert the input signal using a first specific signal output from the first local oscillator and set to a  
15 frequency setting interval of an FD1 step, where  $FD1 = FD/K_1 \times L_1$ , the first local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M_1$  as a modulus, where  $M_1 = F_{s1}/FD \times K_1/L_1$ ; and the second frequency converter is adapted to, if a sampling frequency of the output signal from the first frequency converter is  $F_{s2}$ ,  
20 frequency-convert the output signal from the first frequency converter using a second specific signal output from the second local oscillator and set to a frequency setting interval of an FD2 step, where  $FD2 = (FD \bmod FD1)/K_2$ , the second local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M_2$  as a modulus, where  $M_2 = F_{s2}/(FD \bmod FD1) \times K_2$ .  
25

The digital down-converter with the above-described configuration converts and outputs the input signal sampled at the sampling frequency  $F_{s1}$  into an output signal with a frequency lower than that of the input signal by two frequency conversions. If the desired frequency setting interval of the input signal is FD,  $K_1$ ,  $K_2$  and  $L_1$  are  
30 arbitrary integers and the frequency setting interval FD is above the frequency setting interval FD1 of the first frequency converter and is indivisible by it, the frequency deviation of the output signal from the digital down-converter will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the input

signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the FD1 step, where  $FD1 = FD/K1 \times L1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second local oscillator and set to the frequency setting interval of the FD2 step, where  $FD2 = (FD \bmod FD1)/K2$ . Therefore, the digital down-converter can convert the frequency of the input signal input thereto at the frequency setting interval FD into a desired frequency within the range of an allowable frequency deviation.

10 In accordance with a fourth aspect of the present invention, there is provided a digital down-converter comprising a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert an input signal sampled at a sampling frequency  $Fs1$ , and a second frequency including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the digital down-converter converting and outputting the input signal into an output signal with a frequency lower than that of the input signal by two frequency conversions, wherein: if a desired frequency setting interval of the input signal is FD and  $K1$ ,  $K2$  and  $L1$  are arbitrary integers, the first frequency converter is adapted to frequency-convert the input signal using a first specific signal output from the first local oscillator and set to a frequency setting interval of an FD1 step, where  $FD1 = FD/K1 \times L1$ , the first local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = Fs1/FD \times K1/L1$ ; and the second frequency converter is adapted to, if a sampling frequency of the output signal from the first frequency converter is  $Fs2$ , frequency-convert the output signal from the first frequency converter using a second specific signal output from the second local oscillator and set to a frequency setting interval of an FD2 step, where  $FD2 = (FD1 \bmod FD)/K2$ , the second local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M2$  as a modulus, where  $M2 = Fs2/(FD1 \bmod FD) \times K2$ .

The digital down-converter with the above-described configuration converts and outputs the input signal sampled at the sampling frequency  $Fs1$  into an output signal with a frequency lower than that of the input signal by two frequency conversions. If

the desired frequency setting interval of the input signal is  $FD$ ,  $K1$ ,  $K2$  and  $L1$  are arbitrary integers and the frequency setting interval  $FD$  is below the frequency setting interval  $FD1$  of the first frequency converter and  $FD1$  is indivisible by  $FD$ , the frequency deviation of the output signal from the digital down-converter will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the input signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = FD/K1 \times L1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second local oscillator and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = (FD1 \bmod FD)/K2$ . Therefore, the digital down-converter can convert the frequency of the input signal input thereto at the frequency setting interval  $FD$  into a desired frequency within the range of an allowable frequency deviation.

In accordance with a fifth aspect of the present invention, there is provided a digital down-converter comprising a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert an input signal sampled at a sampling frequency  $Fs1$ , and a second frequency converter including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the digital down-converter converting and outputting the input signal into an output signal with a frequency lower than that of the input signal by two frequency conversions, wherein: if a desired frequency setting interval of the input signal is  $FD$  and  $K1$ ,  $K2$  and  $L1$  are arbitrary integers, the first frequency converter is adapted to frequency-convert the input signal using a first specific signal output from the first local oscillator and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = FD/K1 \times L1$ , the first local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = Fs1/FD \times K1/L1$ ; and the second frequency converter is adapted to, if a sampling frequency of the output signal from the first frequency converter is  $Fs2$ , frequency-convert the output signal from the first frequency converter using a second specific signal output from the second local oscillator and set to a frequency setting interval of an  $FD2$  step, where  $FD2 = FD/K2$ , the second local oscillator outputting the

second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M2$  as a modulus, where  $M2 = F_{s2}/FD \times K2$ .

5 The digital down-converter with the above-described configuration converts and outputs the input signal sampled at the sampling frequency  $F_{s1}$  into an output signal with a frequency lower than that of the input signal by two frequency conversions. If the desired frequency setting interval of the input signal is  $FD$ ,  $K1$ ,  $K2$  and  $L1$  are arbitrary integers, and the frequency setting interval  $FD$  is higher than or equal to the frequency setting interval  $FD1$  of the first frequency converter and is evenly divisible by it, or  $FD$  is lower than  $FD1$  and  $FD1$  is evenly divisible by  $FD$ , first, the first frequency  
10 converter frequency-converts the input signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = FD/K1 \times L1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second  
15 local oscillator and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = FD/K2$ . Therefore, the digital down-converter can convert the frequency of the input signal input thereto at the frequency setting interval  $FD$  into a desired frequency within the range of an allowable frequency deviation.

20 Preferably, in the digital down-converter of the third, fourth, or fifth aspect, the second frequency converter may stop its frequency conversion.

In the case where a multiple of the frequency setting interval  $FD1$  of the first frequency converter is equal to that of the frequency setting interval  $FD$  of the input signal, the digital down-converter with the above-described configuration can convert the frequency of the input signal input thereto at the frequency setting interval  $FD$  into a  
25 desired frequency within the range of an allowable frequency deviation by means of only the first frequency converter.

In accordance with a sixth aspect of the present invention, there is provided a digital up-converter comprising a frequency converter including the NCO of the first aspect as a local oscillator and serving to frequency-convert an input signal, the digital  
30 up-converter converting the input signal into a signal with a frequency higher than that of the input signal and outputting the converted signal as an output signal sampled at the

sampling frequency  $F_s$ , wherein, if a desired frequency setting interval of the output signal is  $FD$  and  $K$  and  $L$  are arbitrary integers, the frequency converter is adapted to frequency-convert the input signal using a specific signal output from the local oscillator and set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ , the local  
 5 oscillator outputting the specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M$  as a modulus, where  $M = F_s/FD \times K/L$ .

In the digital up-converter with the above-described configuration, in order to convert the input signal into a signal with a frequency higher than that of the input signal and output the converted signal as an output signal sampled at the sampling frequency  
 10  $F_s$ , if the desired frequency setting interval of the output signal is  $FD$  and  $K$  and  $L$  are arbitrary integers, the frequency converter frequency-converts the input signal using a frequency signal output from the NCO of the first aspect as the local oscillator and set to the frequency setting interval of the  $dF$  step, where  $dF = FD/K \times L$ . In the case where  
 15 the desired frequency setting interval  $FD$  of the output signal is higher than or equal to the frequency setting interval  $dF$  of the frequency converter and is evenly divisible by it, the digital up-converter can set the frequency setting interval of its output signal to  $FD$ .

In accordance with a seventh aspect of the present invention, there is provided a digital up-converter comprising a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert an input signal,  
 20 and a second frequency converter including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the digital up-converter performing two frequency conversions to convert the input signal into a signal with a frequency higher than that of the input signal and output the converted signal as an output signal sampled at a sampling frequency  $F_{s2}$ ,  
 25 wherein: if a desired frequency setting interval of the output signal is  $FD$  and  $K_1$ ,  $K_2$  and  $L_2$  are arbitrary integers, the second frequency converter is adapted to frequency-convert the output signal from the first frequency converter using a first specific signal output from the second local oscillator and set to a frequency setting interval of an  $FD_2$  step, where  $FD_2 = FD/K_2 \times L_2$ , the second local oscillator outputting  
 30 the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M_2$  as a modulus, where  $M_2 = F_{s2}/FD \times K_2/L_2$ ; and the first frequency converter is adapted to, if a sampling frequency of the input signal is  $F_{s1}$ , frequency-convert the input signal using a second specific signal output from the first

local oscillator and set to a frequency setting interval of an FD1 step, where  $FD1 = (FD \bmod FD2)/K1$ , the first local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of M1 as a modulus, where  $M1 = Fs1/(FD \bmod FD2) \times K1$ .

5           The digital up-converter with the above-described configuration performs two frequency conversions to convert the input signal into a signal with a frequency higher than that of the input signal and output the converted signal as an output signal sampled at the sampling frequency  $Fs2$ . If the desired frequency setting interval of the output signal is FD, K1, K2 and L2 are arbitrary integers and the frequency setting interval FD is above the frequency setting interval FD2 of the second frequency converter and is indivisible by it, the frequency deviation of the output signal from the digital up-converter will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the input signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the FD1 step, where  $FD1 = (FD \bmod FD2)/K1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second local oscillator and set to the frequency setting interval of the FD2 step, where  $FD2 = FD/K2 \times L2$ . Therefore, the digital up-converter can set the frequency setting interval of its output signal to FD.

In accordance with an eighth aspect of the present invention, there is provided a digital up-converter comprising a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert an input signal, and a second frequency converter including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the digital up-converter performing two frequency conversions to convert the input signal into a signal with a frequency higher than that of the input signal and output the converted signal as an output signal sampled at a sampling frequency  $Fs2$ , wherein: if a desired frequency setting interval of the output signal is FD and K1, K2 and L2 are arbitrary integers, the second frequency converter is adapted to frequency-convert the output signal from the first frequency converter using a first specific signal output from the second local oscillator and set to a frequency setting interval of an FD2 step, where  $FD2 = FD/K2 \times L2$ , the second local oscillator outputting

the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M2$  as a modulus, where  $M2 = Fs2/FD \times K2/L2$ ; and the first frequency converter is adapted to, if a sampling frequency of the input signal is  $Fs1$ , frequency-convert the input signal using a second specific signal output from the first local oscillator and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = (FD2 \bmod FD)/K1$ , the first local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = Fs1/(FD2 \bmod FD) \times K1$ .

The digital up-converter with the above-described configuration performs two frequency conversions to convert the input signal into a signal with a frequency higher than that of the input signal and output the converted signal as an output signal sampled at the sampling frequency  $Fs2$ . If the desired frequency setting interval of the output signal is  $FD$ ,  $K1$ ,  $K2$  and  $L2$  are arbitrary integers and the frequency setting interval  $FD$  is below the frequency setting interval  $FD2$  of the second frequency converter and  $FD2$  is indivisible by  $FD$ , the frequency deviation of the output signal from the digital up-converter will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the input signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = (FD2 \bmod FD)/K1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second local oscillator and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = FD/K2 \times L2$ . Therefore, the digital up-converter can set the frequency setting interval of its output signal to  $FD$ .

In accordance with a ninth aspect of the present invention, there is provided a digital up-converter comprising a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert an input signal, and a second frequency converter including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the digital up-converter performing two frequency conversions to convert the input signal into a signal with a frequency higher than that of the input signal and output the converted signal as an output signal sampled at a sampling frequency  $Fs2$ , wherein: if a desired frequency setting interval of the output signal is  $FD$  and  $K1$ ,  $K2$

and  $L2$  are arbitrary integers, the second frequency converter is adapted to frequency-convert the output signal from the first frequency converter using a first specific signal output from the second local oscillator and set to a frequency setting interval of an  $FD2$  step, where  $FD2 = FD/K2 \times L2$ , the second local oscillator outputting  
 5 the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M2$  as a modulus, where  $M2 = Fs2/FD \times K2/L2$ ; and the first frequency converter is adapted to, if a sampling frequency of the input signal is  $Fs1$ , frequency-convert the input signal using a second specific signal output from the first local oscillator and set to a frequency setting interval of an  $FD1$  step, where  $FD1 =$   
 10  $FD/K1$ , the first local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = Fs1/FD \times K1$ .

The digital up-converter with the above-described configuration performs two frequency conversions to convert the input signal into a signal with a frequency higher  
 15 than that of the input signal and output the converted signal as an output signal sampled at the sampling frequency  $Fs2$ . If the desired frequency setting interval of the output signal is  $FD$ ,  $K1$ ,  $K2$  and  $L2$  are arbitrary integers, and the frequency setting interval  $FD$  is higher than or equal to the frequency setting interval  $FD2$  of the second frequency converter and is evenly divisible by it, or  $FD$  is lower than  $FD2$  and  $FD2$  is evenly  
 20 divisible by  $FD$ , first, the first frequency converter frequency-converts the input signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = FD/K1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the  
 25 first aspect as the second local oscillator and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = FD/K2 \times L2$ . Therefore, the digital up-converter can set the frequency setting interval of its output signal to  $FD$ .

Preferably, in the digital up-converter of the seventh, eighth, or ninth aspect, the first frequency converter may stop its frequency conversion.

30 In the case where a multiple of the frequency setting interval  $FD2$  of the second frequency converter is equal to that of the frequency setting interval  $FD$  of the output signal, the digital up-converter with the above-described configuration can set the

frequency setting interval of its output signal to FD by means of only the second frequency converter.

In accordance with a tenth aspect of the present invention, there is provided a receiver comprising a first frequency converter including a first local oscillator and serving to frequency-convert a received signal, the first local oscillator including the NCO of the first aspect operating at the sampling frequency  $F_s$  and a phase locked loop (PLL) circuit having a multiplication ratio  $P$  ( $P$  is an integer) and acting to receive the output signal from the NCO of the first aspect as a reference signal, a second frequency converter including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, and a demodulator for demodulating an output signal from the second frequency converter to extract received data therefrom, the receiver converting the received signal into a baseband received signal with a frequency lower than that of the received signal by two frequency conversions and extracting the received data from the converted baseband received signal, wherein: if a desired frequency setting interval of the received signal is  $FD$  and  $K_1$ ,  $K_2$  and  $L_1$  are arbitrary integers, the first frequency converter is adapted to frequency-convert the received signal using a first specific signal output from the first local oscillator and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K_1 \times L_1$ , the first local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M_1$  as a modulus, where  $M_1 = F_s/FD \times K_1/L_1 \times P$ ; and the second frequency converter is adapted to, if a sampling frequency of the output signal from the first frequency converter is  $F_{s1}$ , frequency-convert the output signal from the first frequency converter using a second specific signal output from the second local oscillator and set to a frequency setting interval of an  $FD_2$  step, where  $FD_2 = (FD \bmod FDP)/K_2$ , the second local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M_2$  as a modulus, where  $M_2 = F_{s1}/(FD \bmod FDP) \times K_2$ .

The receiver with the above-described configuration converts the received signal into a baseband received signal with a frequency lower than that of the received signal by two frequency conversions. If the desired frequency setting interval of the received signal is  $FD$ ,  $K_1$ ,  $K_2$  and  $L_1$  are arbitrary integers and the frequency setting interval  $FD$  is above the frequency setting interval  $FDP$  of the first frequency converter and is

indivisible by it, the deviation of the frequency desired by the demodulator will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the received signal using a frequency signal output from the first local oscillator including the PLL circuit with the multiplication ratio  $P$  and the NCO of the first aspect and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = FDP/P = FD/K1 \times L1/P$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second local oscillator and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = (FD \bmod FDP)/K2$ . Therefore, the receiver can accurately convert the frequency of the received signal input thereto at the frequency setting interval  $FD$  into that desired by the demodulator.

In accordance with an eleventh aspect of the present invention, there is provided a receiver comprising a first frequency converter including a first local oscillator and serving to frequency-convert a received signal, the first local oscillator including the NCO of the first aspect operating at the sampling frequency  $F_s$  and a PLL circuit (having a multiplication ratio  $P$  ( $P$  is an integer) and acting to receive the output signal from the NCO of the first aspect as a reference signal, a second frequency converter (for example, the frequency converter 12 of the sixth embodiment or the frequency converter 85 of the seventh embodiment) including the NCO of the first aspect as a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, and a demodulator for demodulating an output signal from the second frequency converter to extract received data therefrom, the receiver converting the received signal into a baseband received signal with a frequency lower than that of the received signal by two frequency conversions and extracting the received data from the converted baseband received signal, wherein: if a desired frequency setting interval of the received signal is  $FD$  and  $K1$ ,  $K2$  and  $L1$  are arbitrary integers, the first frequency converter is adapted to frequency-convert the received signal using a first specific signal output from the first local oscillator and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K1 \times L1$ , the first local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = F_s/FD \times K1/L1 \times P$ ; and the second frequency converter is adapted to, if a sampling frequency of the output signal from the first frequency converter is  $F_{s1}$ , frequency-convert the output signal from the first frequency

converter using a second specific signal output from the second local oscillator and set to a frequency setting interval of an FD2 step, where  $FD2 = (FDP \bmod FD)/K2$ , the second local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of M2 as a modulus, 5 where  $M2 = Fs1/(FDP \bmod FD) \times K2$ .

The receiver with the above-described configuration converts the received signal into a baseband received signal with a frequency lower than that of the received signal by two frequency conversions. If the desired frequency setting interval of the received signal is FD, K1, K2, and L1 are arbitrary integers and the frequency setting interval FD 10 is below the frequency setting interval FDP of the first frequency converter and FDP is indivisible by FD, the deviation of the frequency desired by the demodulator will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the received signal using a frequency signal output from the first local oscillator including the PLL circuit with the multiplication ratio P and the NCO of 15 the first aspect and set to the frequency setting interval of the FD1 step, where  $FD1 = FDP/P = FD/K1 \times L1/P$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second local oscillator and set to the frequency setting interval of the FD2 step, where  $FD2 = (FDP \bmod 20 FD)/K2$ . Therefore, the receiver can accurately convert the frequency of the received signal input thereto at the frequency setting interval FD into that desired by the demodulator.

In accordance with a twelfth aspect of the present invention, there is provided a receiver comprising a first frequency converter including a first local oscillator and 25 serving to frequency-convert a received signal, the first local oscillator including the NCO of the first aspect operating at the sampling frequency Fs and a PLL circuit (having a multiplication ratio P (P is an integer) and acting to receive the output signal from the NCO of the first aspect as a reference signal, a second frequency converter including the NCO of the first aspect as a second local oscillator and serving to 30 secondarily frequency-convert an output signal from the first frequency converter, and a demodulator for demodulating an output signal from the second frequency converter to extract received data therefrom, the receiver converting the received signal into a baseband received signal with a frequency lower than that of the received signal by two

frequency conversions and extracting the received data from the converted baseband received signal, wherein: if a desired frequency setting interval of the received signal is  $FD$  and  $K1$ ,  $K2$  and  $L1$  are arbitrary integers, the first frequency converter is adapted to frequency-convert the received signal using a first specific signal output from the first local oscillator and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K1 \times L1$ , the first local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = Fs/FD \times K1/L1 \times P$ ; and the second frequency converter is adapted to, if a sampling frequency of the output signal from the first frequency converter is  $Fs1$ , frequency-convert the output signal from the first frequency converter using a second specific signal output from the second local oscillator and set to a frequency setting interval of an  $FD2$  step, where  $FD2 = FD/K2$ , the second local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M2$  as a modulus, where  $M2 = Fs1/FD \times K2$ .

The receiver with the above-described configuration converts the received signal into a baseband received signal with a frequency lower than that of the received signal by two frequency conversions. If the desired frequency setting interval of the received signal is  $FD$ ,  $K1$ ,  $K2$  and  $L1$  are arbitrary integers, and the frequency setting interval  $FD$  is higher than or equal to the frequency setting interval  $FDP$  of the first frequency converter and is evenly divisible by it, or  $FD$  is lower than  $FDP$  and  $FDP$  is evenly divisible by  $FD$ , first, the first frequency converter frequency-converts the received signal using a frequency signal output from the first local oscillator including the PLL circuit with the multiplication ratio  $P$  and the NCO of the first aspect and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = FDP/P = FD/K1 \times L1/P$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the NCO of the first aspect as the second local oscillator and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = FD/K2$ . Therefore, the receiver can accurately convert the frequency of the received signal input thereto at the frequency setting interval  $FD$  into that desired by the demodulator.

Preferably, in the receiver of the tenth, eleventh, or twelfth aspect, the second frequency converter may stop its frequency conversion.

In the case where a multiple of the frequency setting interval FD1 of the first frequency converter is equal to that of the frequency setting interval FD of the received signal, the receiver with the above-described configuration can accurately convert the frequency of the received signal input thereto at the frequency setting interval FD into that desired by the demodulator by means of only the first frequency converter.

In accordance with a thirteenth aspect of the present invention, there is provided a transmitter comprising a modulator for modulating and outputting a baseband transmit signal based on transmit data, a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert the output signal from the modulator, a second frequency converter including a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the second local oscillator including the NCO of the first aspect operating at the sampling frequency  $F_s$  and a PLL circuit having a multiplication ratio  $P$  ( $P$  is an integer) and acting to receive the output signal from the NCO of the first aspect as a reference signal, the transmitter converting and outputting the baseband transmit signal into a transmit signal with a frequency higher than that of the baseband transmit signal by two frequency conversions, wherein: if a desired frequency setting interval of the transmit signal is  $FD$  and  $K_1$ ,  $K_2$  and  $L_2$  are arbitrary integers, the second frequency converter is adapted to frequency-convert the output signal from the first frequency converter using a first specific signal output from the second local oscillator and set to a frequency setting interval of an FDP step, where  $FDP = FD/K_2 \times L_2$ , the second local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M_2$  as a modulus, where  $M_2 = F_s/FD \times K_2/L_2 \times P$ ; and the first frequency converter is adapted to, if a sampling frequency of the output signal from the modulator is  $F_{s1}$ , frequency-convert the output signal from the modulator using a second specific signal output from the first local oscillator and set to a frequency setting interval of an FD1 step, where  $FD1 = (FD \bmod FDP)/K_1$ , the first local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M_1$  as a modulus, where  $M_1 = F_{s1}/(FD \bmod FDP) \times K_1$ .

The transmitter with the above-described configuration converts and outputs the baseband transmit signal into a transmit signal with a frequency higher than that of the baseband transmit signal by two frequency conversions.

If the desired frequency setting interval of the transmit signal is  $FD$ ,  $K1$ ,  $K2$  and  $L2$  are arbitrary integers and the frequency setting interval  $FD$  is above the frequency setting interval  $FDP$  of the second frequency converter and is indivisible by it, the frequency deviation of the transmit signal from the transmitter will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the baseband transmit signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = (FD \bmod FDP)/K1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the second local oscillator including the PLL circuit with the multiplication ratio  $P$  and the NCO of the first aspect and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = FDP/P = FD/K2 \times L2/P$ . Therefore, the transmitter can accurately convert the frequency of the baseband transmit signal from the modulator into a target transmit signal frequency.

In accordance with a fourteenth aspect of the present invention, there is provided a transmitter comprising a modulator for modulating and outputting a baseband transmit signal based on transmit data, a first frequency converter including the NCO of the first aspect as a first local oscillator and serving to frequency-convert the output signal from the modulator, a second frequency converter including a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the second local oscillator including the NCO of the first aspect operating at the sampling frequency  $F_s$  and a PLL circuit having a multiplication ratio  $P$  ( $P$  is an integer) and acting to receive the output signal from the NCO of the first aspect as a reference signal, the transmitter converting and outputting the baseband transmit signal into a transmit signal with a frequency higher than that of the baseband transmit signal by two frequency conversions, wherein: if a desired frequency setting interval of the transmit signal is  $FD$  and  $K1$ ,  $K2$  and  $L2$  are arbitrary integers, the second frequency converter is adapted to frequency-convert the output signal from the first frequency converter using a first specific signal output from the second local oscillator and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K2 \times L2$ , the second local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M2$  as a modulus, where  $M2 = F_s/FD \times K2/L2 \times P$ ; and the first frequency converter is adapted to, if a sampling frequency

of the output signal from the modulator is  $F_{s1}$ , frequency-convert the output signal from the modulator using a second specific signal output from the first local oscillator and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = (FDP \bmod FD)/K1$ , the first local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = F_{s1}/(FDP \bmod FD) \times K1$ .

The transmitter with the above-described configuration converts and outputs the baseband transmit signal into a transmit signal with a frequency higher than that of the baseband transmit signal by two frequency conversions.

If the desired frequency setting interval of the transmit signal is  $FD$ ,  $K1$ ,  $K2$ , and  $L2$  are arbitrary integers and the frequency setting interval  $FD$  is below the frequency setting interval  $FD2$  of the second frequency converter and  $FD2$  is indivisible by  $FD$ , the frequency deviation of the transmit signal from the transmitter will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the baseband transmit signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = (FDP \bmod FD)/K1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the second local oscillator including the PLL circuit with the multiplication ratio  $P$  and the NCO of the first aspect and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = FDP/P = FD/K2 \times L2/P$ . Therefore, the transmitter can accurately convert the frequency of the baseband transmit signal from the modulator into a target transmit signal frequency.

In accordance with a fifteenth aspect of the present invention, there is provided a transmitter comprising a modulator for modulating and outputting a baseband transmit signal based on transmit data, a first frequency converter including the NCO of the first aspect as a first local and serving to frequency-convert the output signal from the modulator, a second frequency converter including a second local oscillator and serving to secondarily frequency-convert an output signal from the first frequency converter, the second local oscillator including the NCO of the first aspect operating at the sampling frequency  $F_s$  and a PLL circuit having a multiplication ratio  $P$  ( $P$  is an integer) and acting to receive the output signal from the NCO of the first aspect as a reference signal,

the transmitter converting and outputting the baseband transmit signal into a transmit signal with a frequency higher than that of the baseband transmit signal by two frequency conversions, wherein: if a desired frequency setting interval of the transmit signal is  $FD$  and  $K1$ ,  $K2$  and  $L2$  are arbitrary integers, the second frequency converter is adapted to frequency-convert the output signal from the first frequency converter using a first specific signal output from the second local oscillator and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K2 \times L2$ , the second local oscillator outputting the first specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M2$  as a modulus, where  $M2 = F_s/FD \times K2/L2 \times P$ ; and the first frequency converter is adapted to, if a sampling frequency of the output signal from the modulator is  $F_{s1}$ , frequency-convert the output signal from the modulator using a second specific signal output from the first local oscillator and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = FD/K1$ , the first local oscillator outputting the second specific signal by accumulating the phase difference data by a modulo operation taking a nearest integer of  $M1$  as a modulus, where  $M1 = F_{s1}/FD \times K1$ .

The transmitter with the above-described configuration converts and outputs the baseband transmit signal into a transmit signal with a frequency higher than that of the baseband transmit signal by two frequency conversions.

If the desired frequency setting interval of the transmit signal is  $FD$ ,  $K1$ ,  $K2$ , and  $L2$  are arbitrary integers, and the frequency setting interval  $FD$  is higher than or equal to the frequency setting interval  $FD2$  of the second frequency converter and is evenly divisible by it, or  $FD$  is lower than  $FD2$  and  $FD2$  is evenly divisible by  $FD$ , the frequency deviation of the transmit signal from the transmitter will exceed an allowable range. For this reason, first, the first frequency converter frequency-converts the baseband transmit signal using a frequency signal output from the NCO of the first aspect as the first local oscillator and set to the frequency setting interval of the  $FD1$  step, where  $FD1 = FD/K1$ . Then, the second frequency converter secondarily frequency-converts the output signal from the first frequency converter using a frequency signal output from the second local oscillator including the PLL circuit with the multiplication ratio  $P$  and the NCO of the first aspect and set to the frequency setting interval of the  $FD2$  step, where  $FD2 = FDP/P = FD/K2 \times L2/P$ . Therefore, the transmitter can accurately convert the

frequency of the baseband transmit signal from the modulator into a target transmit signal frequency.

Preferably, in the transmitter of the thirteenth, fourteenth, or fifteenth aspect, the first frequency converter may stop its frequency conversion.

5           In the case where a multiple of the frequency setting interval FD2 of the second frequency converter is equal to that of the frequency setting interval FD of the transmit signal, the transmitter with the above-described configuration can accurately convert the frequency of the baseband transmit signal from the modulator into that of a target transmit signal by means of only the second frequency converter.

## 10                           **BRIEF DESCRIPTION OF THE DRAWINGS**

The above and other objects, features, and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

15           Fig. 1 is a block diagram illustrating the configuration of a numerical control oscillator according to a first embodiment of the present invention;

          Fig. 2 is a graph illustrating a comparison of simulation results of spurious characteristics between a conventional numerical control oscillator and the numerical control oscillator of the first embodiment;

20           Fig. 3 is a block diagram illustrating the configuration of an embodiment of a digital down-converter using the numerical control oscillator of the first embodiment;

          Fig. 4 is a block diagram illustrating the configuration of an embodiment of a digital up-converter using the numerical control oscillator of the first embodiment;

25           Fig. 5 is a block diagram illustrating the configuration of an alternative embodiment of the digital down-converter using the numerical control oscillator of the first embodiment;

          Fig. 6 is a block diagram illustrating the configuration of an alternative embodiment of the digital up-converter using the numerical control oscillator of the first embodiment;

30           Fig. 7 is a block diagram illustrating the configuration of an embodiment of a receiver using the numerical control oscillator of the first embodiment;

Fig. 8 is a block diagram illustrating the configuration of an alternative embodiment of the receiver using the numerical control oscillator of the first embodiment; and

Fig. 9 is a block diagram illustrating the configuration of a transmitter using the  
5 numerical control oscillator of the first embodiment.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail herein below with reference to the annexed drawings. In the following description, a detailed description of known functions and configurations incorporated herein will be omitted  
10 when it may make the subject matter of the present invention rather unclear.

Fig. 1 is a block diagram illustrating the configuration of a numerical control oscillator (NCO) of the first embodiment. As illustrated in Fig. 1, the NCO comprises a phase accumulator 1 for accumulating input phase difference data to generate phase data, and a memory, preferably a read only memory (ROM), 2 for storing a phase/amplitude conversion table to output amplitude data corresponding to the phase data generated by the phase accumulator 1.

In detail, on the assumption that a sampling frequency of an output signal from the NCO is  $F_s$ , the upper limit of a desired frequency setting interval of the output signal is  $F_D$ , and  $K$  and  $L$  are arbitrary integers, the phase accumulator 1 includes a phase register 1a for storing and outputting the phase data, and a phase calculator 1b for  
15 adding or subtracting the input phase difference data and the phase data from the phase register 1a to or from each other by a modulo operation taking the nearest integer of  $M$  as a modulus, where  $M = F_s/F_D \times K/L$ . Therefore, the phase accumulator 1 accumulates the phase difference data as an input signal to the NCO to generate the phase data.

The ROM 2 has its address terminal connected to an output terminal of the phase accumulator 1 by  $j$ -bit wiring, where  $j = \log_2 M$  (where,  $j$  is rounded up to the  
20 nearest integer), and stores the phase/amplitude conversion table, which includes  $M$  amplitude data. Therefore, the ROM 2 outputs the amplitude data corresponding to the phase data, input from the phase accumulator 1 to the address terminal, through its data terminal as the output signal of the NCO. As a result, the NCO of the present

embodiment provides its output signal set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ .

For example, assuming that the sampling frequency  $F_s$  of the output signal from the NCO is 153.6MHz, the upper limit  $FD$  of the desired frequency setting interval of the output signal is 200KHz, and  $K$  and  $L$  are 1s, the phase calculator 1b adds or subtracts the input phase difference data and the phase data from the phase register 1a to or from each other by a modulo operation taking  $M = "768"$  as a modulus, where  $M = F_s/FD \times K/L = 153.6[\text{MHz}]/200[\text{KHz}] = 768$ .

Also, the address terminal of the ROM 2 is connected to the output terminal of the phase accumulator 1 by the  $j$ -bit wiring, where  $j = \log_2 M = \log_2 768 \doteq 9.58 = 10$  (where,  $j$  is rounded up to the nearest integer), namely, 10-bit wiring.

Therefore, the word length of the ROM 2 and the phase word length of the phase calculator 1b become equal, and as a result there is no need to requantize an address word length (the word length of the ROM 2) from the phase calculator 1b. Therefore, it is possible to realize a low-spurious NCO which has no error  $e^p$  resulting from requantization and provides its output signal based on only low-capacity amplitude data of 768 words necessary for the modulo operation based on the modulus of "768" under the condition that the sampling frequency  $F_s$  of the output signal is 153.6MHz and the frequency setting interval  $dF$  is  $FD/K \times L = 200\text{KHz}$ .

Further, the NCO with the above-described configuration can have settings corresponding to respective communication systems (for example, a W-CDMA mobile phone system, an IS-95 mobile phone system and an IEEE 802.11a wireless LAN system), including the above-described exemplary values, as shown in the below table 1.

【Table 1】

No.	FD[KHz]	F <sub>s</sub> [MHz]	dF[KHz]	K	L	M
W-CDMA						
1	200	61.44	40	5	1	1536
2	200	61.44	80	5	2	768
3	200	92.16	40	5	1	2304
4	200	122.88	40	5	1	3072

5	200	153.6	200	1	1	768
6	200	153.6	1600	1	8	96
7	200	184.32	200	5	1	4608
IS-95 Band Class 0						
8	30	98.304	6	5	1	16384
9	30	98.304	12	5	2	8192
IEEE 802.11a						
10	20000	100	20000	1	1	5
11	20000	200	20000	1	1	10

As one example of the above table 1, assuming that the sampling frequency  $F_s$  of the output signal from the NCO is 61.44MHz, the upper limit  $FD$  of the desired frequency setting interval of the output signal is 200KHz,  $K$  is 5, and  $L$  is 1, the output signal is provided based on only low-capacity amplitude data of 1536 words necessary for a modulo operation taking  $M = "1536"$  as a modulus by the phase calculator 1b, where  $M = F_s/FD \times K/L = 61.44[\text{MHz}]/200[\text{KHz}] \times 5 = 1536$ . That is, it is possible to realize a low-spurious NCO which provides its output signal based on only low-capacity amplitude data under the condition that the sampling frequency  $F_s$  of the output signal is 61.44MHz and the frequency setting interval  $dF$  is  $FD/K \times L = 200[\text{KHz}]/5 = 40[\text{KHz}]$ .

Fig. 2 is a graph illustrating a comparison of simulation results of spurious characteristics between a conventional NCO that performs a modulo operation taking  $2^j$  as a modulus (a parameter is represented by a phase word length  $j$  and the number of amplitude data in the phase/amplitude conversion table) and the NCO of the first embodiment (a parameter is represented by only the number of amplitude data in the phase/amplitude conversion table) under the above-described condition, wherein the axis of abscissa represents an amplitude data bit length output from the ROM 2, the axis of ordinate represents a spurious, and the number of amplitude data in the phase/amplitude conversion table stored in the ROM 2 represents a parameter. As illustrated in Fig. 2, in the case where the NCO of the present embodiment makes the word length of the ROM 2 shorter to use amplitude data of, for example, 384 words, 192 words or 96 words, the spurious characteristics thereof are severely worsened. However, as long as the NCO generates phase data by adding or subtracting the input phase difference data and the phase data from the phase register 1a to or from each other by a modulo operation taking the nearest integer of  $M$  as a modulus, where  $M = F_s/FD \times K/L$ , namely,  $M = 768$

under the above condition, it can obtain the same spurious characteristics as those of a conventional NCO that performs a modulo operation taking  $2^{20}$  as a modulus and requires amplitude data of about 1M words.

Next, a description will be given of examples of applications of the NCO of the first embodiment with reference to the accompanying drawings. For example, the NCO of the first embodiment may be used in a digital down-converter as shown in Fig. 3.

Fig. 3 is a block diagram illustrating the configuration of an embodiment of a digital down-converter 11 using the NCO of the first embodiment. As illustrated in Fig. 3, the digital down-converter 11 comprises a frequency converter 12 for frequency-converting an input signal of a center frequency  $F_{if1}$  to obtain a complex signal (zero IF signal) of a center frequency  $F_{if2} = 0[\text{Hz}]$ . The frequency converter 12 includes a local oscillator 12a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_c$  (containing a real component " $C(t) = \cos(2\pi \times F_c \times t)$ " and an imaginary component " $-S(t) = -\sin(2\pi \times F_c \times t)$ " whose phase is 90 degrees ahead of that of the real component), and multipliers 12b and 12c for multiplying the input signal by the real and imaginary components of the complex local signal generated by the local oscillator 12a, respectively.

A decimator 13 decimates the complex signal from the frequency converter 12. To this end, the decimator 13 includes real and imaginary decimators 13a and 13b each for multiplying a sampling frequency  $F_{s1}$  of a corresponding one of real and imaginary components of the complex signal by  $1/N$  to convert it into a sampling frequency  $F_{s2} = F_{s1}/N$ . A roll-off filter 14 band-limits the complex signal decimated by the decimator 13 to a target signal band to output the resulting complex signal (I,Q). To this end, the roll-off filter 14 includes a real filter 14a and an imaginary filter 14b.

For example, assuming that a desired frequency setting interval  $FD$  of an input signal is evenly divisible by a frequency setting interval  $dF$  of the frequency converter 12, the digital down-converter 11 is operated in the following manner. In this case, if  $K$  and  $L$  are arbitrary integers, the frequency converter 12 sets phase difference data  $\phi$  to the local oscillator 12a using the NCO of the first embodiment to a value of  $\phi = F_c/dF = F_c/FD \times K/L$ . Then, the frequency converter 12 accurately converts an input signal of a

center frequency  $F_{if1}$  into a complex signal of a center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_c$  output from the local oscillator 12a and set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ . Here, the local oscillator 12a outputs the complex local signal of the frequency  $F_c$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M$  as a modulus, where  $M =$   
 5  $F_{s1}/FD \times K/L$ .

More specifically, assuming that a sampling frequency  $F_{s1}$  of an input signal is 153.6MHz, a desired frequency setting interval  $FD$  of the input signal is 200KHz, a center frequency  $F_{if1}$  of the input signal is 36.4MHz and  $K = L = 1$ , the frequency  
 10 converter 12 sets phase difference data  $\phi$  to the local oscillator 12a using the NCO of the first embodiment to  $\phi = F_c/dF = F_c/FD \times K/L = 36.4[\text{MHz}]/200[\text{KHz}] = 182$ . Then, the frequency converter 12 accurately converts the input signal of the center frequency  $F_{if1}$  into a complex signal (zero IF signal) of a center frequency  $F_{if2} = 0[\text{Hz}]$  using a complex local signal of a frequency  $F_c = 36.4[\text{MHz}]$  output from the local oscillator 12a  
 15 and set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L = 200[\text{KHz}]$ . Here, the local oscillator 12a outputs the complex local signal of the frequency  $F_c$  by accumulating the phase difference data by a modulo operation taking  $M = 768$  as a modulus, where  $M = F_{s1}/FD \times K/L = 153.6[\text{MHz}]/200[\text{KHz}] = 768$ .

The NCO of the first embodiment may also be used in a digital up-converter as  
 20 illustrated in Fig. 4.

Fig. 4 is a block diagram illustrating the configuration of an embodiment of a digital up-converter using the NCO of the first embodiment. As illustrated in Fig. 4, the digital up-converter comprises a roll-off filter 21 for band-limiting an input complex signal (containing baseband signal components I and Q) of a center frequency  $F_{if1} =$   
 25  $0[\text{Hz}]$  to a target signal band. The roll-off filter 21 includes a real filter 21a and an imaginary filter 21b. An interpolator 22 interpolates the complex signal band-limited by the roll-off filter 21. To this end, the interpolator 22 includes real and imaginary interpolators 22a and 22b each for multiplying a sampling frequency  $F_{s1}$  of a corresponding one of real and imaginary components of the complex signal by  $N$  to  
 30 convert it into a sampling frequency  $F_{s2} = F_{s1} \times N$ .

A frequency converter 23 frequency-converts an output signal from the interpolator 22 to output a real signal of a target center frequency  $F_{if2}$ . To this end, the frequency converter 23 includes a local oscillator 23a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_c$  (containing a real component “ $C(t) = \cos(2\pi F_c t)$ ” and an imaginary component “ $S(t) = \sin(2\pi F_c t)$ ” whose phase is 90 degrees delayed from that of the real component), multipliers 23b and 23c for multiplying real and imaginary components of the output signal from the interpolator 22 by the real and imaginary components of the complex local signal generated by the local oscillator 23a, respectively, and a subtracter 23d for subtracting output signals from the multipliers 23b and 23c from each other.

For example, assuming that a desired frequency setting interval  $FD$  of an output signal is evenly divisible by a frequency setting interval  $dF$  of the frequency converter 23, the digital up-converter is operated in the following manner. In this case, if  $K$  and  $L$  are arbitrary integers, the frequency converter 23 sets phase difference data  $\phi$  to the local oscillator 23a using the NCO of the first embodiment to a value of  $\phi = F_c/dF = F_c/FD \times K/L$ . Then, the frequency converter 23 accurately converts a baseband signal of a center frequency  $F_{if1}$  into a complex signal of a target center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_c$  output from the local oscillator 23a and set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ . Here, the local oscillator 23a outputs the complex local signal of the frequency  $F_c$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M$  as a modulus, where  $M = Fs2/FD \times K/L$ .

In detail, assuming that a sampling frequency  $Fs2$  of an output signal is 153.6MHz, a desired frequency setting interval  $FD$  of the output signal is 200KHz, a center frequency  $F_{if2}$  of the output signal is 72.8MHz and  $K = L = 1$ , the frequency converter 23 sets phase difference data  $\phi$  to the local oscillator 23a using the NCO of the first embodiment to  $\phi = F_c/dF = F_c/FD \times K/L = 72.8[\text{MHz}]/200[\text{KHz}] = 364$ . Then, the frequency converter 23 accurately converts a baseband signal of a center frequency  $F_{if1} = 0[\text{Hz}]$  into a complex signal of a target center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_c = 72.8[\text{MHz}]$  output from the local oscillator 23a and set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L = 200[\text{KHz}]$ . Here, the local oscillator 23a outputs the complex local signal of the frequency  $F_c$  by

accumulating the phase difference data by a modulo operation taking  $M = 768$  as a modulus, where  $M = F_s/2/F_D \times K/L = 153.6[\text{MHz}]/200[\text{KHz}] = 768$ .

Next, a description will be given of the configuration of an alternative embodiment of the digital down-converter using the NCO of the first embodiment, which comprises first and second frequency converters each including the NCO as a local oscillator and serves to convert and output an input signal into a signal with a frequency lower than that of the input signal by two frequency conversions.

Fig. 5 is a block diagram illustrating the configuration of the alternative embodiment of the digital down-converter using the numerical control oscillator of the first embodiment. As illustrated in Fig. 5, the digital down-converter comprises a frequency converter 31 for frequency-converting an input signal of a center frequency  $F_{if1}$  to obtain a complex signal of a center frequency  $F_{if2}$ . The frequency converter 31 includes a local oscillator 31a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_{c1}$  (containing a real component " $C1(t) = \cos(2\pi \times F_{c1} \times t)$ " and an imaginary component " $-S1(t) = -\sin(2\pi \times F_{c1} \times t)$ " whose phase is 90 degrees ahead of that of the real component), and multipliers 31b and 31c for multiplying the input signal by the real and imaginary components of the complex local signal generated by the local oscillator 31a, respectively.

A decimator 32 decimates the complex signal from the frequency converter 31. To this end, the decimator 32 includes real and imaginary decimators 32a and 32b each for multiplying a sampling frequency  $F_{s1}$  of a corresponding one of real and imaginary components of the complex signal by  $1/N$  to convert it into a sampling frequency  $F_{s2} = F_{s1}/N$ . A frequency converter 33 frequency-converts the complex signal decimated by the decimator 32 to obtain a complex signal of a center frequency  $F_{if3}$ . The frequency converter 33 includes a local oscillator 33a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_{c2}$  (containing a real component " $C2(t) = \cos(2\pi \times F_{c2} \times t)$ " and an imaginary component " $-S2(t) = -\sin(2\pi \times F_{c2} \times t)$ " whose phase is 90 degrees ahead of that of the real component), and multipliers 33b, 33c, 33d, and 33e, a subtracter 33f and an adder 33g for performing multiplication, subtraction and addition operations with respect to the complex signal decimated by the

decimator 32 and the complex local signal generated by the local oscillator 33a, respectively.

A roll-off filter 34 band-limits the complex signal from the frequency converter 33 to a target signal band to output the resulting complex signal (I,Q) of the center frequency  $F_{if3}$ . The roll-off filter 34 includes a real filter 34a and an imaginary filter 34b.

For example, assuming that a sampling frequency of an input signal is  $F_{s1}$ , and a desired frequency setting interval  $FD$  of the input signal is above a frequency setting interval  $FD1$  of the frequency converter 31 and is indivisible by it, the digital down-converter is operated in the following manner. In this case, if  $K1$ ,  $K2$ , and  $L1$  are arbitrary integers, the frequency converter 31 sets phase difference data  $\phi1$  to the local oscillator 31a using the NCO of the first embodiment to a value of  $\phi1 = F_{c1}/FD1 = F_{c1}/FD \times K1/L1$ . Then, the frequency converter 31 converts an input signal of a center frequency  $F_{if1}$  into a complex signal of a center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_{c1}$  output from the local oscillator 31a and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = FD/K1 \times L1$ . Here, the local oscillator 31a outputs the complex local signal of the frequency  $F_{c1}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M1$  as a modulus, where  $M1 = F_{s1}/FD \times K1/L1$ .

Also, the frequency converter 33 sets phase difference data  $\phi2$  to the local oscillator 33a using the NCO of the first embodiment to a value of  $\phi2 = F_{c2}/FD2 = F_{c2}/(FD \bmod FD1) \times K2$ . Then, the frequency converter 33 converts the complex signal of the center frequency  $F_{if2}$  into a complex signal of a center frequency  $F_{if3}$  using a complex local signal of a frequency  $F_{c2}$  output from the local oscillator 33a and set to a frequency setting interval of an  $FD2$  step, where  $FD2 = (FD \bmod FD1)/K2$ . Here, the local oscillator 33a outputs the complex local signal of the frequency  $F_{c2}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M2$  as a modulus, where  $M2 = F_{s2}/(FD \bmod FD1) \times K2$ .

More specifically, assuming that a sampling frequency  $F_{s1}$  of an input signal is 98.304MHz, a desired frequency setting interval  $FD$  of the input signal is 30KHz, a center frequency  $F_{if1}$  of the input signal is 13.742MHz,  $K1 = 15$  and  $L1 = 8$ , the frequency converter 31 sets phase difference data  $\phi1$  to the local oscillator 31a using the

NCO of the first embodiment to  $\phi_1 = F_{c1}/FD_1 = F_{c1}/FD \times K_1/L_1 = 13.728[\text{MHz}]/30[\text{KHz}] \times 15/8 = 858$ . The frequency converter 31 accurately converts the input signal of the center frequency  $F_{if1}$  into a complex signal of a center frequency  $F_{if2} = 14[\text{Hz}]$  using a complex local signal of a frequency  $F_{c1} = 13.728[\text{MHz}]$  output from the local oscillator 31a and set to a frequency setting interval of an  $FD_1$  step, where  $FD_1 = FD/K_1 \times L_1 = 30[\text{KHz}]/15 \times 8 = 16[\text{KHz}]$ . Here, the local oscillator 31a outputs the complex local signal of the frequency  $F_{c1}$  by accumulating the phase difference data by a modulo operation taking  $M_1 = 6144$  as a modulus, where  $M_1 = F_{s1}/FD \times K_1/L_1 = 98.304[\text{MHz}]/30[\text{KHz}] \times 15/8 = 6144$ .

Also, assuming that a decimation rate  $N$  of the decimator 32 is 10 and  $K_2 = 7$ , the frequency converter 33 sets phase difference data  $\phi_2$  to the local oscillator 33a using the NCO of the first embodiment to  $\phi_2 = F_{c2}/FD_2 = F_{c2}/(FD \bmod FD_1) \times K_2 = 14[\text{KHz}]/(30[\text{KHz}] \bmod 16[\text{KHz}]) \times 7 = 7$ . Then, the frequency converter 33 accurately converts the complex signal of the center frequency  $F_{if2}$  into a complex signal (zero IF signal) of a center frequency  $F_{if3} = 0[\text{Hz}]$  using a complex local signal of a frequency  $F_{c2}$  output from the local oscillator 33a and set to a frequency setting interval of an  $FD_2$  step, where  $FD_2 = (FD \bmod FD_1)/K_2 = (30[\text{KHz}] \bmod 16[\text{KHz}])/7 = 2[\text{KHz}]$ . Here, the local oscillator 33a outputs the complex local signal of the frequency  $F_{c2}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M_2$ , 4915, as a modulus, where  $M_2 = F_{s2}/(FD \bmod FD_1) \times K_2 = 9.8304[\text{MHz}]/(30[\text{KHz}] \bmod 16[\text{KHz}]) \times 7$ .

However, for example, assuming that a desired frequency setting interval  $FD$  of an input signal is below a frequency setting interval  $FD_1$  of the frequency converter 31 and  $FD_1$  is indivisible by  $FD$ , the frequency converter 31 sets phase difference data  $\phi_1$  to the local oscillator 31a using the NCO of the first embodiment to a value of  $\phi_1 = F_{c1}/FD_1 = F_{c1}/FD \times K_1/L_1$ . Then, the frequency converter 31 converts an input signal of a center frequency  $F_{if1}$  into a complex signal of a center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_{c1}$  output from the local oscillator 31a and set to a frequency setting interval of an  $FD_1$  step, where  $FD_1 = FD/K_1 \times L_1$ . Here, the local oscillator 31a outputs the complex local signal of the frequency  $F_{c1}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M_1$  as a modulus, where  $M_1 = F_{s1}/FD \times K_1/L_1$ .

Also, the frequency converter 33 sets phase difference data  $\phi_2$  to the local oscillator 33a using the NCO of the first embodiment to a value of  $\phi_2 = F_{c2}/FD_2 = F_{c2}/(FD_1 \bmod FD) \times K_2$ . Then, the frequency converter 33 converts the complex signal of the center frequency  $F_{if2}$  into a complex signal of a center frequency  $F_{if3}$  using a complex local signal of a frequency  $F_{c2}$  output from the local oscillator 33a and set to a frequency setting interval of an  $FD_2$  step, where  $FD_2 = (FD_1 \bmod FD)/K_2$ . Here, the local oscillator 33a outputs the complex local signal of the frequency  $F_{c2}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M_2$  as a modulus, where  $M_2 = F_{s2}/(FD_1 \bmod FD) \times K_2$ .

Conversely, for example, assuming that a desired frequency setting interval  $FD$  of an input signal is higher than or equal to a frequency setting interval  $FD_1$  of the frequency converter 31 and is evenly divisible by it, or that  $FD$  is lower than  $FD_1$  and  $FD_1$  is evenly divisible by  $FD$ , the frequency converter 31 sets phase difference data  $\phi_1$  to the local oscillator 31a using the NCO of the first embodiment to a value of  $\phi_1 = F_{c1}/FD_1 = F_{c1}/FD \times K_1/L_1$ . Then, the frequency converter 31 converts an input signal of a center frequency  $F_{if1}$  into a complex signal of a center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_{c1}$  output from the local oscillator 31a and set to a frequency setting interval of an  $FD_1$  step, where  $FD_1 = FD/K_1 \times L_1$ . Here, the local oscillator 31a outputs the complex local signal of the frequency  $F_{c1}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M_1$  as a modulus, where  $M_1 = F_{s1}/FD \times K_1/L_1$ .

Also, the frequency converter 33 sets phase difference data  $\phi_2$  to the local oscillator 33a using the NCO of the first embodiment to a value of  $\phi_2 = F_{c2}/FD_2 = F_{c2}/FD \times K_2$ . Then, the frequency converter 33 converts the complex signal of the center frequency  $F_{if2}$  into a complex signal of a center frequency  $F_{if3}$  using a complex local signal of a frequency  $F_{c2}$  output from the local oscillator 33a and set to a frequency setting interval of an  $FD_2$  step, where  $FD_2 = FD/K_2$ . Here, the local oscillator 33a outputs the complex local signal of the frequency  $F_{c2}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M_2$  as a modulus, where  $M_2 = F_{s2}/FD \times K_2$ .

However, in the case where a multiple of the frequency setting interval  $FD_1$  of the frequency converter 31 is equal to that of the frequency setting interval  $FD$  of the

input signal, the digital down-converter with the above-described configuration can convert the frequency of the input signal input thereto at the frequency setting interval FD into a desired frequency within the range of an allowable frequency deviation by means of only the frequency converter 31. In this case, the frequency conversion by the frequency converter 33 may be stopped.

Further, the digital down-converter with the above-stated configuration can have various settings of the respective parameters, including the above-described exemplary values, as shown in the below tables 2 to 5. The tables 2 and 3 show examples of settings of the respective parameters in a W-CDMA system, the table 4 shows examples of settings of the respective parameters in an IS-95 Band (Class 0) system, and the table 5 shows examples of settings of the respective parameters in an IEEE 802.11a system.

It should be noted that, in the tables, examples having no description of settings of the parameters associated with the frequency converter 33 are realizable by the digital down-converter configuration of Fig. 3 and those parameters are again readable as the corresponding parameters.

【Table 2】

No.	Fifa [MHz]	Fifl [MHz]	FD [KHz]	FDl [KHz]	Fsl [MHz]	Fcl [MHz]	K1	L1	M1	$\Delta\phi$
1	190.00	5.680	200.0	40.0	61.440	5.680	5	1	153 6	142
2	190.00	5.680	200.0	40.0	92.160	5.680	5	1	230 4	142
3	190.00	-55.760	200.0	40.0	122.880	-55.76 0	5	1	307 2	-1394
4	189.60	36.000	200.0	200.0	153.600	36.000	1	1	768	180
5	189.80	36.200	200.0	200.0	153.600	36.200	1	1	768	181
6	190.00	36.400	200.0	200.0	153.600	36.400	1	1	768	182
7	190.15	36.550	200.0	200.0	153.600	36.400	1	1	768	182
8	190.20	36.600	200.0	200.0	153.600	36.600	1	1	768	183
9	190.35	36.750	200.0	200.0	153.600	36.600	1	1	768	183
10	190.40	36.800	200.0	200.0	153.600	36.800	1	1	768	184
11	189.80	36.200	200.0	1600.0	153.600	35.200	1	8	96	22

12	190.00	36.400	200.0	1600.0	153.600	35.200	1	8	96	22
13	190.20	36.600	200.0	1600.0	153.600	35.200	1	8	96	22
14	190.00	5.680	200.0	40.0	184.320	5.680	5	1	460 8	142

【Table 3】

No.	Fif2 [KHz]	Fs2 [MHz]	FD2 [KHz]	Fc2 [KHz]	K2	M2	$\Delta\phi$ 2
1	-	-	-	-	-	-	-
2	-	-	-	-	-	-	-
3	-	-	-	-	-	-	-
4	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-
6	-	-	-	-	-	-	-
7	150.0	30.72	50.00 0	150.10	4	614	3
8	-	-	-	-	-	-	-
9	150.0	30.72	50.00 0	150.10	4	614	3
10	-	-	-	-	-	-	-
11	1000. 0	30.72	40.00 0	1000.0 0	5	768	25
12	1200. 0	30.72	40.00 0	1200.0 0	5	768	30
13	1400. 0	30.72	40.00 0	1400.0 0	5	768	35
14	-	-	-	-	-	-	-

【Table 4】

No.	Fifa [MHz]	Fifl [MHz]	FD [KHz]	FDl [KHz]	Fsl [MHz]	Fcl [MHz]	K1	L1	M1	$\Delta\phi$ 1
1	210.35	13.742	30.0	16.0	98.304	13.728	15	8	6144	858
2	210.38	13.772	30.0	16.0	98.304	13.760	15	8	6144	860

3	210.41	13.802	30.0	16.0	98.304	13.792	15	8	6144	862
4	210.35	53.064	30.0	11.3	157.286	53.055	8	3	1398 1	471 6
5	210.38	53.094	30.0	11.3	157.286	53.089	8	3	1398 1	471 9
6	210.41	53.124	30.0	11.3	157.286	53.123	8	3	1398 1	472 2

No.	Fif2 [KHz]	Fs2 [MHz]	FD2 [KHz]	Fc2 [KHz]	K2	M2	$\Delta\phi$ 2
1	14.00	9.8304	2.000	14.00	7	4915	7
2	12.00	9.8304	2.000	12.00	7	4915	6
3	10.00	9.8304	2.000	10.00	7	4915	5
4	8.60	9.8304	1.250	8.75	6	7864	7
5	4.90	9.8304	1.250	5.00	6	7864	4
6	1.10	9.8304	1.250	1.25	6	7864	1

【Table 5】

No.	Fifa [MHz]	Fif1 [MHz]	FD [KHz]	FD1 [KHz]	Fs1 [MHz]	Fc1 [MHz]	K1	L1	M1	$\Delta\phi$ 1
1	180.00	-20.000	100.0	100.0	100.000	-20.00 0	1	1	1000	-200
2	179.80	-20.200	200.0	400.0	200.000	-20.40 0	1	2	500	-51
3	180.00	-20.000	200.0	400.0	200.000	-20.00 0	1	2	500	-50
4	180.20	-19.800	200.0	400.0	200.000	-20.00 0	1	2	500	-50

No.	Fif2 [KHz]	Fs2 [MHz]	FD2 [KHz]	Fc2 [KHz]	K2	M2	$\Delta\phi$ 2
1	-	-	-	-	-	-	-
2	200.0	20	200.00 0	200.00	1	100	1

3	-	-	-	-	-	-	-
4	200.0	20	200.00 0	200.00	1	100	1

In the digital-down converter of the present embodiment, where the frequency setting interval FD1 of the frequency converter 31 is settable at a step lower than or equal to the desired frequency setting interval FD of the input signal, each frequency can be input by merely changing the setting of frequency data (phase difference data) to the NCO of the frequency converter 31. Therefore, a data setting time of a controller that controls the digital down-converter can be reduced by half compared with a conventional digital down-converter requiring the setting of data to both frequency converters and the frequency data to the NCO can be computed in a simpler manner.

More specifically, for example, where a frequency is set at a 200KHz step between a lower IF limit and an upper IF limit on the assumption that the lower IF limit is 180MHz, the upper IF limit is 200MHz and the sampling frequency  $F_{s1} = 153.6\text{MHz}$ , the digital down-converter in which the frequency setting interval dF of the input signal is 200KHz can set the phase difference data  $\phi$  to 132 for the lower IF limit, and to 232 for the upper IF limit by incrementing the phase difference data  $\phi$  by "1" whenever changing the IF by 200KHz.

Additionally, the NCO of the first embodiment may be used in a digital up-converter as illustrated in Fig. 6. In the case where a center frequency  $F_{if3}$  of an output signal is indivisible by a desired frequency setting interval FD of the output signal, the digital up-converter comprises a first frequency converter, and a second frequency converter including the NCO as a local oscillator, and serves to perform two frequency conversions to convert an input signal into a signal with a frequency higher than that of the input signal and output the converted signal as a signal sampled at a sampling frequency  $F_s$ .

Fig. 6 is a block diagram illustrating the configuration of an alternative embodiment of the digital up-converter using the NCO of the first embodiment. As illustrated in Fig. 6, the digital up-converter comprises a roll-off filter 41 for band-limiting an input complex signal (containing baseband signal components I and Q)

of a center frequency  $F_{f1} = 0[\text{Hz}]$  to a target signal band. The roll-off filter 41 includes a real filter 41a and an imaginary filter 41b.

A frequency converter 42 frequency-converts an output signal from the roll-off filter 41 to obtain a complex signal of a center frequency  $F_{f2}$ . The frequency converter 42 includes a local oscillator 42a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_{c1}$  (containing a real component " $C1(t) = \cos(2\pi x F_{c1} t)$ " and an imaginary component " $S1(t) = \sin(2\pi x F_{c1} t)$ " whose phase is 90 degrees delayed from that of the real component), and multipliers 42b, 42c, 42d and 42e, a subtracter 42f and an adder 42g for performing multiplication, subtraction and addition operations with respect to the output signal from the roll-off filter 41 and the complex local signal generated by the local oscillator 42a, respectively.

An interpolator 43 interpolates the complex signal from the frequency converter 42. To this end, the interpolator 43 includes real and imaginary interpolators 43a and 43b each for multiplying a sampling frequency  $F_{s1}$  of a corresponding one of real and imaginary components of the complex signal by  $N$  to convert it into a sampling frequency  $F_{s2} = F_{s1} \times N$ . A frequency converter 44 frequency-converts an output signal from the interpolator 43 to output a real signal of a target center frequency  $F_{f3}$ . The frequency converter 44 includes a local oscillator 44a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_{c2}$  (containing a real component " $C2(t) = \cos(2\pi x F_{c2} t)$ " and an imaginary component " $S2(t) = \sin(2\pi x F_{c2} t)$ " whose phase is 90 degrees delayed from that of the real component), multipliers 44b and 44c for multiplying real and imaginary components of the output signal from the interpolator 43 by the real and imaginary components of the complex local signal generated by the local oscillator 44a, respectively, and a subtracter 44d for subtracting output signals from the multipliers 44b and 44c from each other.

For example, assuming that a desired frequency setting interval  $FD$  of an output signal is above a frequency setting interval  $FD2$  of the frequency converter 44 and is indivisible by it, the digital up-converter is operated in the following manner. In this case, if  $K1$ ,  $K2$ , and  $L2$  are arbitrary integers, the frequency converter 42 sets phase difference data  $\phi1$  to the local oscillator 42a using the NCO of the first embodiment to a value of  $\phi1 = F_{c1}/FD1 = F_{c1}/(FD \bmod FD2) \times K1$ . Then, the frequency converter 42 converts a baseband signal of a center frequency  $F_{f1}$  into a complex signal of a center frequency

Fif2 using a complex local signal of a frequency Fc1 output from the local oscillator 42a and set to a frequency setting interval of an FD1 step, where  $FD1 = (FD \bmod FD2)/K1$ . The local oscillator 42a outputs the complex local signal of the frequency Fc1 by accumulating the phase difference data by a modulo operation taking the nearest integer of M1 as a modulus, where  $M1 = Fs2/(FD \bmod FD2) \times K1$ .

Also, the frequency converter 44 sets phase difference data  $\phi2$  to the local oscillator 44a using the NCO of the first embodiment to a value of  $\phi2 = Fc2/FD2 = Fc2/FD \times K2/L2$ . The frequency converter 44 converts the complex signal of the center frequency Fif2 into a complex signal of a center frequency Fif3 using a complex local signal of a frequency Fc2 output from the local oscillator 44a and set to a frequency setting interval of an FD2 step, where  $FD2 = FD/K2 \times L2$ . Here, the local oscillator 44a outputs the complex local signal of the frequency Fc2 by accumulating the phase difference data by a modulo operation taking the nearest integer of M2 as a modulus, where  $M2 = Fs2/FD \times K2/L2$ .

However, for example, assuming that a desired frequency setting interval FD of an output signal is below a frequency setting interval FD2 of the frequency converter 44 and FD2 is indivisible by FD, the frequency converter 42 sets phase difference data  $\phi1$  to the local oscillator 42a using the NCO of the first embodiment to a value of  $\phi1 = Fc1/FD1 = Fc1/(FD2 \bmod FD) \times K1$ . The frequency converter 42 converts a baseband signal of a center frequency Fif1 into a complex signal of a center frequency Fif2 using a complex local signal of a frequency Fc1 output from the local oscillator 42a and set to a frequency setting interval of an FD1 step, where  $FD1 = (FD2 \bmod FD)/K1$ . Here, the local oscillator 42a outputs the complex local signal of the frequency Fc1 by accumulating the phase difference data by a modulo operation taking the nearest integer of M1 as a modulus, where  $M1 = Fs2/(FD2 \bmod FD) \times K1$ .

Also, the frequency converter 44 sets phase difference data  $\phi2$  to the local oscillator 44a using the NCO of the first embodiment to a value of  $\phi2 = Fc2/FD2 = Fc2/FD \times K2/L2$ . Then, the frequency converter 44 converts the complex signal of the center frequency Fif2 into a complex signal of a center frequency Fif3 using a complex local signal of a frequency Fc2 output from the local oscillator 44a and set to a frequency setting interval of an FD2 step, where  $FD2 = FD/K2 \times L2$ . The local oscillator 44a outputs the complex local signal of the frequency Fc2 by accumulating the phase

difference data by a modulo operation taking the nearest integer of  $M2$  as a modulus, where  $M2 = Fs2/FD \times K2/L2$ .

Alternatively, for example, assuming that a desired frequency setting interval  $FD$  of an output signal is higher than or equal to a frequency setting interval  $FD2$  of the frequency converter 44 and is evenly divisible by it, or that  $FD$  is lower than  $FD2$  and  $FD2$  is evenly divisible by  $FD$ , the digital up-converter is operated in the following manner. In this case, the frequency converter 42 sets phase difference data  $\phi1$  to the local oscillator 42a using the NCO of the first embodiment to a value of  $\phi1 = Fc1/FD1 = Fc1/FD \times K1$ . The frequency converter 42 converts a baseband signal of a center frequency  $Fif1$  into a complex signal of a center frequency  $Fif2$  using a complex local signal of a frequency  $Fc1$  output from the local oscillator 42a and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = FD/K1$ . Here, the local oscillator 42a outputs the complex local signal of the frequency  $Fc1$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M1$  as a modulus, where  $M1 = Fs2/FD \times K1$ .

Also, the frequency converter 44 sets phase difference data  $\phi2$  to the local oscillator 44a using the NCO of the first embodiment to a value of  $\phi2 = Fc2/FD2 = Fc2/FD \times K2/L2$ . Then, the frequency converter 44 converts the complex signal of the center frequency  $Fif2$  into a complex signal of a center frequency  $Fif3$  using a complex local signal of a frequency  $Fc2$  output from the local oscillator 44a and set to a frequency setting interval of an  $FD2$  step, where  $FD2 = FD/K2 \times L2$ . The local oscillator 44a outputs the complex local signal of the frequency  $Fc2$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M2$  as a modulus, where  $M2 = Fs2/FD \times K2/L2$ .

However, in the case where a multiple of the frequency setting interval  $FD2$  of the frequency converter 44 is equal to that of the frequency setting interval  $FD$  of the output signal, the digital up-converter with the above-described configuration can set the frequency setting interval of its output signal to  $FD$  by means of only the frequency converter 44. In this case, the frequency conversion by the frequency converter 42 may be stopped.

In the digital-up converter of the present embodiment, in the case where the frequency setting interval FD2 of the frequency converter 44 is settable at a step lower than or equal to the desired frequency setting interval FD of the output signal, each frequency can be input by merely changing the setting of frequency data (phase difference data) to the NCO of the frequency converter 44. Therefore, a data setting time of a controller that controls the digital up-converter can be reduced by half compared with a conventional digital up-converter requiring the setting of data to both frequency converters and the frequency data to the NCO can be computed in a simpler manner.

Fig. 7 is a block diagram illustrating the configuration of an embodiment of a receiver using the NCO of the first embodiment. As illustrated in Fig. 7, the receiver comprises a local oscillator 51 including the NCO 51a of the first embodiment, a digital to analog converter (DAC) 51b for digital/analog-converting an output signal from the NCO 51a, and a PLL circuit 51c for receiving an output signal from the DAC 51b as a reference signal. The receiver further comprises a mixer 52 for frequency-converting a received signal (real signal) of a center frequency  $F_{rf}$  into an analog intermediate frequency (IF) signal of a center frequency  $F_{ifa}$  on the basis of an analog local signal (real signal " $C(t) = \cos(2\pi \times F_{cp} \times t)$ ") of a frequency  $F_{cp}$  output from the local oscillator 51.

Assuming that a multiplication ratio of the PLL circuit 51c is  $P$  and an output frequency of the NCO 51a is  $F_{c1}$ , the local oscillator 51 outputs an analog local signal of a frequency  $F_{cp} = F_{rf} - F_{ifa} = F_{c1} \times P$ . Also, a frequency setting step FDP of the analog local signal (frequency setting interval of the mixer 52) is a multiplication of a frequency setting step FD of the NCO 51a by  $P$ .

A band pass filter 53 has a pass frequency band characteristic corresponding to a frequency band of the analog IF signal and acts to extract the analog IF signal from the mixer 52 and output it to an analog to digital converter (ADC) 54.

The ADC 54 quantizes the analog IF signal from the band pass filter 53 and generates a "Sub-Nyquist sampled" digital IF signal of a center frequency  $F_{if2}$ .

The digital down-converter 11 of Fig. 3 is used to convert an output signal from the ADC 54 into a complex signal (I,Q) of a frequency desired by a demodulator 55 and output the converted complex signal to the demodulator 55. The demodulator 55 demodulates the output signal from the digital down-converter 11 to extract received data therefrom.

For example, assuming that a desired frequency setting interval FD of a received signal is above a frequency setting interval FDP of the mixer 52 and is indivisible by it, the receiver is operated in the following manner. In this case, if K1, K2 and L1 are arbitrary integers, the mixer 52 sets phase difference data  $\phi 1$  to the NCO 51a of the first embodiment operating at a sampling frequency Fs to a value of  $\phi 1 = Fc1/FD1 = Fc1/FD \times K1/L1$ . The mixer 52 converts a received signal of a center frequency Frf into an analog IF signal of a center frequency Fifa using an analog local signal of a frequency Fcp output from the local oscillator 51 and set to a frequency setting interval of an FDP step, where  $FDP = FD/K1 \times L1$ . Here, the local oscillator 51 outputs the analog local signal of the frequency Fcp by accumulating the phase difference data by a modulo operation taking the nearest integer of M1 as a modulus, where  $M1 = Fs/FD \times K1/L1 \times P$ .

Also, the frequency converter 12 sets phase difference data  $\phi 2$  to the local oscillator 12a using the NCO of the first embodiment to a value of  $\phi 2 = Fc2/FD2 = Fc2/(FD \bmod FDP) \times K2$ . Then, the frequency converter 12 converts a digital IF signal of a center frequency Fif2 and sampling frequency Fs1, generated by Sub-Nyquist sampling the analog IF signal of the center frequency Fifa by the ADC 54, into a complex signal of a frequency desired by the demodulator 55 using a complex local signal of a frequency Fc2 output from the local oscillator 12a and set to a frequency setting interval of an FD2 step, where  $FD2 = (FD \bmod FDP)/K2$ . The local oscillator 12a outputs the complex local signal of the frequency Fc2 by accumulating the phase difference data by a modulo operation taking the nearest integer of M2 as a modulus, where  $M2 = Fs1/(FD \bmod FDP) \times K2$ .

However, for example, assuming that a desired frequency setting interval FD of a received signal is below a frequency setting interval FDP of the mixer 52 and FDP is indivisible by FD, the mixer 52 sets phase difference data  $\phi 1$  to the NCO 51a of the first embodiment operating at a sampling frequency Fs to a value of  $\phi 1 = Fc1/FD1 = Fc1/FD \times K1/L1$ . The mixer 52 converts a received signal of a center frequency Frf into

an analog IF signal of a center frequency  $F_{if1}$  using an analog local signal of a frequency  $F_{cp}$  output from the local oscillator 51 and set to a frequency setting interval of an FDP step, where  $FDP = FD/K1 \times L1$ . Here, the local oscillator 51 outputs the analog local signal of the frequency  $F_{cp}$  by accumulating the phase difference data by a modulo  
 5 operation taking the nearest integer of  $M1$  as a modulus, where  $M1 = F_s/FD \times K1/L1 \times P$ .

Also, the frequency converter 12 sets phase difference data  $\phi_2$  to the local oscillator 12a using the NCO of the first embodiment to a value of  $\phi_2 = F_{c2}/FD2 = F_{c2}/(FDP \bmod FD) \times K2$ . The frequency converter 12 converts a digital IF signal of a center frequency  $F_{if2}$  and sampling frequency  $F_{s1}$ , generated by Sub-Nyquist sampling  
 10 the analog IF signal of the center frequency  $F_{if1}$  by the ADC 54, into a complex signal of a frequency desired by the demodulator 55 using a complex local signal of a frequency  $F_{c2}$  output from the local oscillator 12a and set to a frequency setting interval of an  $FD2$  step, where  $FD2 = (FDP \bmod FD)/K2$ . The local oscillator 12a outputs the complex local signal of the frequency  $F_{c2}$  by accumulating the phase difference data by  
 15 a modulo operation taking the nearest integer of  $M2$  as a modulus, where  $M2 = F_{s1}/(FDP \bmod FD) \times K2$ .

Alternatively, for example, assuming that a desired frequency setting interval  $FD$  of a received signal is higher than or equal to a frequency setting interval  $FDP$  of the mixer 52 and is evenly divisible by it, or that  $FD$  is lower than  $FDP$  and  $FDP$  is evenly  
 20 divisible by  $FD$ , the mixer 52 sets phase difference data  $\phi_1$  to the NCO 51a of the first embodiment operating at a sampling frequency  $F_s$  to a value of  $\phi_1 = F_{c1}/FD1 = F_{c1}/FD \times K1/L1$ . The mixer 52 converts a received signal of a center frequency  $F_{rf}$  into an analog IF signal of a center frequency  $F_{if1}$  using an analog local signal of a frequency  $F_{cp}$  output from the local oscillator 51 and set to a frequency setting interval of an FDP  
 25 step, where  $FDP = FD/K1 \times L1$ . The local oscillator 51 outputs the analog local signal of the frequency  $F_{cp}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M1$  as a modulus, where  $M1 = F_s/FD \times K1/L1 \times P$ .

Also, the frequency converter 12 sets phase difference data  $\phi_2$  to the local oscillator 12a using the NCO of the first embodiment to a value of  $\phi_2 = F_{c2}/FD2 = F_{c2}/FD \times K2$ . Then, the frequency converter 12 converts a digital IF signal of a center  
 30 frequency  $F_{if2}$  and sampling frequency  $F_{s1}$ , generated by Sub-Nyquist sampling the analog IF signal of the center frequency  $F_{if1}$  by the ADC 54, into a complex signal of a

frequency desired by the demodulator 55 using a complex local signal of a frequency Fc2 output from the local oscillator 12a and set to a frequency setting interval of an FD2 step, where  $FD2 = FD/K2$ . Here, the local oscillator 12a outputs the complex local signal of the frequency Fc2 by accumulating the phase difference data by a modulo  
 5 operation taking the nearest integer of M2 as a modulus, where  $M2 = Fs1/FD \times K2$ .

On the other hand, in the case where a multiple of the frequency setting interval FDP of the mixer 52 is equal to that of the frequency setting interval FD of the received signal, the receiver with the above-described configuration can convert the frequency of the received signal input thereto at the frequency setting interval FD into that desired by  
 10 the demodulator 55 by means of only the mixer 52. In this case, the frequency conversion by the frequency converter 12 may be stopped.

Further, the receiver with the above-stated configuration can have various settings of the respective parameters as shown in the below tables 6 to 9. The tables 6 and 7 show examples of settings of the respective parameters in a W-CDMA system, the  
 15 table 8 shows examples of settings of the respective parameters in an IS-95 Band (Class 0) system, and the table 9 shows examples of settings of the respective parameters in an IEEE 802.11a system.

【Table 6】

No.	Frf [MHz]	Fcp [MHz]	P	FD [KHz]	FDP [KHz]	Fs [MHz]	FD1 [KHz ]	Fc1 [MHz]	K1	L1
1	2257.50	2068.00	200	200.0	4000.0	61.440	20.0	10.340	1	20
2	2257.50	2068.00	100	200.0	4000.0	92.160	40.0	20.680	1	20
3	2257.50	2068.00	100	200.0	4000.0	122.88 0	40.0	20.680	1	20
4	2247.50	2060.00	100	200.0	5000.0	153.60 0	50.0	20.600	1	25
5	2252.50	2065.00	100	200.0	5000.0	153.60 0	50.0	20.650	1	25
6	2257.50	2070.00	100	200.0	5000.0	153.60 0	50.0	20.700	1	25
7	2257.52	2070.00	100	200.0	5000.0	153.60	50.0	20.700	1	25

						0				
8	2262.50	2075.00	100	200.0	5000.0	153.60 0	50.0	20.750	1	25
9	2262.54	2075.00	100	200.0	5000.0	153.60 0	50.0	20.750	1	25
10	2267.50	2080.00	100	200.0	5000.0	153.60 0	50.0	20.800	1	25
11	2257.50	2066.40	128	200.0	2400.0	153.60 0	18.8	16.144	1	12
12	2257.50	2066.40	128	200.0	2400.0	153.60 0	18.8	16.144	1	12
13	2257.50	2066.40	128	200.0	2400.0	153.60 0	18.8	16.144	1	12
14	2257.50	2070.00	50	200.0	5000.0	150.00 0	100.0	41.400	1	25

【Table 7】

No	M1	$\Delta\phi_1$	Fifa [MHz]	Fi2 [MHz ]	Fs1 [MHz ]	FD2 [KHz]	Fc2 [MHz ]	K2	M2	$\Delta\phi_2$
1	3072	517	189.50	35.90	153.6	100.00 0	35.90	2	153 6	359
2	2304	517	189.50	35.90	153.6	100.00 0	35.90	2	153 6	359
3	3072	517	189.50	35.90	153.6	100.00 0	35.90	2	153 6	359
4	3072	412	187.50	33.90	153.6	100.00 0	33.90	2	153 6	339
5	3072	413	187.50	33.90	153.6	100.00 0	33.90	2	153 6	339
6	3072	414	187.50	33.90	153.6	100.00 0	33.90	2	153 6	339
7	3072	414	187.52	33.92	153.6	20.000	33.92	10	768 0	1696
8	3072	415	187.50	33.90	153.6	100.00	33.90	2	153	339

						0			6	
9	3072	415	187.54	33.94	153.6	20.000	33.94	10	768 0	1697
10	3072	416	187.50	33.90	153.6	100.00 0	33.90	2	153 6	339
11	8192	861	191.10	37.50	153.6	100.00 0	37.50	2	153 6	375
12	8192	861	191.10	37.50	153.6	100.00 0	37.50	2	153 6	375
13	8192	861	191.10	37.50	153.6	100.00 0	37.50	2	153 6	375
14	1500	414	187.50	33.90	153.6	100.00 0	33.90	2	153 6	339

【Table 8】

No.	Frf [MHz]	Fcp [MHz]	P	FD [KHz ]	FDP [KHz]	Fs [MHz]	FD1 [KHz]	Fc1 [MHz]	K1	L1
1	869.97	679.68	50	30.0	960.0	98.304	19.2	13.594	1	32
2	870.00	679.68	50	30.0	960.0	98.304	19.2	13.594	1	32
3	870.03	679.68	50	30.0	960.0	98.304	19.2	13.594	1	32
4	869.97	679.68	50	30.0	960.0	157.28 6	19.2	13.594	1	32
5	870.00	679.68	50	30.0	960.0	157.28 6	19.2	13.594	1	32
6	870.03	679.68	50	30.0	960.0	157.28 6	19.2	13.594	1	32

No.	M1	$\Delta\phi 1$	Fif1 [MHz ]	Fif2 [MHz ]	Fs1 [MHz]	FD2 [KHz]	Fc2 [MHz]	K2	M2	$\Delta\phi 2$
1	5120	708	190.2 9	33.00	157.28 6	3.750	33.00	8	4194 3	880 1
2	5120	708	190.3 2	33.03	157.28 6	3.750	33.03	8	4194 3	880 9

3	5120	708	190.3 5	33.06	157.28 6	3.750	33.06	8	4194 3	881 7
4	8192	708	190.2 9	33.00	157.28 6	3.750	33.00	8	4194 3	880 1
5	8192	708	190.3 2	33.03	157.28 6	3.750	33.03	8	4194 3	880 9
6	8192	708	190.3 5	33.06	157.28 6	3.750	33.06	8	4194 3	881 7

【Table 9】

No.	Frf [MHz]	Fcp [MHz]	P	FD [KHz] ]	FDP [KHz]	Fs [MHz]	FD1 [KHz]	Fc1 [MHz]	K1	L1
1	5200.0 0	5010.0 0	200	100.0	10000. 0	100.0	50.0	25.050	1	100
2	5180.0 0	4990.0 0	128	200.0	10000. 0	200.0	78.1	38.984	1	50
3	5200.0 0	5010.0 0	128	200.0	10000. 0	200.0	78.1	39.141	1	50
4	5220.0 0	5030.0 0	128	200.0	10000. 0	200.0	78.1	39.297	1	50

No.	M1	$\Delta\phi_1$	Fifa [MHz] ]	Fif2 [MHz] ]	Fs1 [MHz]	FD2 [KHz]	Fc2 [MHz]	K2	M2	$\Delta\phi_2$
1	2000	501	190.0 0	-10.0 0	100	100.00 0	-10.00	1	1000	-100
2	2560	499	190.0 0	-10.0 0	200	200.00 0	-10.00	1	1000	-50
3	2560	501	190.0 0	-10.0 0	200	200.00 0	-10.00	1	1000	-50
4	2560	503	190.0 0	-10.0 0	200	200.00 0	-10.00	1	1000	-50

In the receiver of the present embodiment, where the frequency setting interval FDP of the mixer 52 is settable at a step lower than or equal to the desired frequency setting interval FD of the received signal, each frequency can be input by merely changing the setting of frequency data (phase difference data) to the NCO of the local oscillator 51. Therefore, a data setting time of a controller that controls the receiver can be reduced compared with a conventional receiver and the frequency data to the NCO can be computed in a simpler manner.

Fig. 8 is a block diagram illustrating the configuration of an alternative embodiment of the receiver using the NCO of the first embodiment, wherein a quadrature demodulator 82 is used instead of the mixer 52 of the receiver illustrated in Fig. 7 to quadrature-demodulate an analog version of a received signal. Referring to Fig. 8, the receiver comprises a local oscillator 81 including the NCO 81a of the first embodiment, a DAC 81b for digital/analog-converting an output signal from the NCO 81a, and a PLL circuit 81c for receiving an output signal from the DAC 81b as a reference signal. The quadrature demodulator 82 frequency-converts a received signal (real signal) of a center frequency  $F_{rf}$  into an analog IF complex signal of a center frequency  $F_{ifa}$  on the basis of an analog local signal (containing a real component " $C1(t) = \cos(2\pi \times F_{cp} \times t)$ " and an imaginary component " $-S1(t) = -\sin(2\pi \times F_{cp} \times t)$ " whose phase is 90 degrees ahead of that of the real component) of a frequency  $F_{cp}$  output from the local oscillator 81. To this end, the quadrature demodulator 82 includes a real mixer 82a and an imaginary mixer 82b.

Assuming that a multiplication ratio of the PLL circuit 81c is  $P$  and an output frequency of the NCO 81a is  $F_{c1}$ , the local oscillator 81 outputs an analog local signal of a frequency  $F_{cp} = F_{rf} - F_{ifa} = F_{c1} \times P$ . Also, a frequency setting step FDP of the analog local signal (frequency setting interval of the quadrature demodulator 82) is a multiplication of a frequency setting step FD of the NCO 81a by  $P$ .

A band pass filter 83 has a pass frequency band characteristic corresponding to a frequency band of the analog IF complex signal and acts to extract the analog IF complex signal from the quadrature demodulator 82 and output it to an ADC 84. To this end, the band pass filter 83 includes a real band pass filter 83a and an imaginary band pass filter 83b.

The ADC 84 quantizes the analog IF complex signal from the band pass filter 83 and generates a digital IF signal of a center frequency  $F_{if2}$ . The ADC 84 includes a real ADC 84a and an imaginary ADC 84b.

A frequency converter 85 frequency-converts an output signal from the ADC 84.

5 The frequency converter 85 includes a local oscillator 85a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_{c2}$  (containing a real component " $C2(t) = \cos(2\pi \times F_{c2} \times t)$ " and an imaginary component " $-S2(t) = -\sin(2\pi \times F_{c2} \times t)$ " whose phase is 90 degrees ahead of that of the real component), and multipliers 85b, 85c, 85d, and 85e, a subtracter 85f and an adder 85g for performing

10 multiplication, subtraction and addition operations with respect to the output signal from the ADC 84 and the complex local signal generated by the local oscillator 85a, respectively.

A decimator 86 decimates a complex signal from the frequency converter 85.

The decimator 86 includes real and imaginary decimators 86a and 86b each for

15 multiplying a sampling frequency  $F_{s1}$  of a corresponding one of real and imaginary components of the complex signal by  $1/N$  to convert it into a sampling frequency  $F_{s2} = F_{s1}/N$ . A roll-off filter 87 band-limits an output signal from the decimator 86 to a target signal band and outputs the resulting complex signal (I,Q) of the frequency desired by the demodulator 55 thereto. The roll-off filter 87 includes a real filter 87a and an

20 imaginary filter 87b.

In the above-described receiver, the NCO 81a, local oscillator 81, local oscillator 85a and frequency converter 85 perform the same operations as those of the NCO 51a, local oscillator 51, local oscillator 12a and frequency converter 12 in the receiver previously stated with reference to Fig. 7 on the basis of the relations between the

25 desired frequency setting interval  $FD$  of the received signal and the frequency setting interval  $FDP$  of the quadrature demodulator 82, respectively.

However, in the case where a multiple of the frequency setting interval  $FDP$  of the quadrature demodulator 82 is equal to that of the frequency setting interval  $FD$  of the received signal, the receiver with the above-described configuration can convert the

30 frequency of the received signal input thereto at the frequency setting interval  $FD$  into

that desired by the demodulator by means of only the quadrature demodulator 82. In this case, the frequency conversion by the frequency converter 85 may be stopped.

Further, the receiver with the above-stated configuration can have various settings of the respective parameters as shown in the below tables 10 to 13. The tables 10 and 11 show examples of settings of the respective parameters in a W-CDMA system, the table 12 shows examples of settings of the respective parameters in an IS-95 Band (Class 0) system, and the table 13 shows examples of settings of the respective parameters in an IEEE 802.11a system.

【Table 10】

No.	Frf [MHz]	Fcp [MHz]	P	FD [KHz]	FDP [KHz]	Fs [MHz]	FD1 [KHz]	Fc1 [MHz]	K1	L1
1	2257.50	2256.00	200.0	200.0	4000.0	61.440	20.0	11.280	1	20
2	2257.50	2256.00	100.0	200.0	4000.0	92.160	40.0	22.560	1	20
3	2257.50	2256.00	100.0	200.0	4000.0	122.880	40.0	22.560	1	20
4	2247.50	2250.00	100.0	200.0	5000.0	153.600	50.0	22.500	1	25
5	2252.50	2255.00	100.0	200.0	5000.0	153.600	50.0	22.550	1	25
6	2257.50	2260.00	100.0	200.0	5000.0	153.600	50.0	22.600	1	25
7	2257.52	2260.00	100.0	200.0	5000.0	153.600	50.0	22.600	1	25
8	2262.50	2265.00	100.0	200.0	5000.0	153.600	50.0	22.650	1	25
9	2262.54	2265.00	100.0	200.0	5000.0	153.600	50.0	22.650	1	25
10	2267.50	2270.00	100.0	200.0	5000.0	153.600	50.0	22.700	1	25
11	2257.50	2258.40	128.0	200.0	2400.0	153.600	18.8	17.644	1	12

12	2257.50	2258.40	128.0	200.0	2400.0	153.60 0	18.8	17.644	1	12
13	2257.50	2258.40	128.0	200.0	2400.0	153.60 0	18.8	17.644	1	12
14	2257.50	2260.00	50.0	200.0	5000.0	150.00 0	100.0	45.200	1	25

【Table 11】

No	M1	$\Delta\phi_1$	Fifa [MHz]	Fif2 [MHz ]	Fs1 [MHz ]	FD2 [KHz]	Fc2 [MHz ]	K2	M2	$\Delta\phi_2$
1	3072	564	1.50	1.50	30.72	25.000	1.50	8	122 9	60
2	2304	564	1.50	1.50	30.72	25.000	1.50	8	122 9	60
3	3072	564	1.50	1.50	30.72	25.000	1.50	8	122 9	60
4	3072	450	-2.50	-2.50	30.72	20.000	-2.50	10	153 6	-125
5	3072	451	-2.50	-2.50	30.72	20.000	-2.50	10	153 6	-125
6	3072	452	-2.50	-2.50	30.72	20.000	-2.50	10	153 6	-125
7	3072	452	-2.48	-2.48	30.72	20.000	-2.48	10	153 9	-124
8	3072	453	-2.50	-2.50	30.72	20.000	-2.50	10	153 6	-125
9	3072	453	-2.46	-2.46	30.72	20.000	-2.46	10	153 6	-123
10	3072	454	-2.50	-2.50	30.72	20.000	-2.50	10	153 6	-125
11	8192	941	-0.90	-0.90	30.72	33.333	-0.90	6	922	-27
12	8192	941	-0.90	-0.90	30.72	33.333	-0.90	6	922	-27
13	8192	941	-0.90	-0.90	30.72	33.333	-0.90	6	922	-27
14	1500	452	-2.50	-2.50	30.72	20.000	-2.50	10	153	-125

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【Table 12】

No.	Frf [MHz]	Fcp [MHz]	P	FD [KHz ]	FDP [KHz]	Fs [MHz]	FD1 [KHz]	Fc1 [MHz]	K1	L1
1	869.97	869.76	50	30.0	960.0	98.304	19.2	17.395	1	32
2	870.00	869.76	50	30.0	960.0	98.304	19.2	17.395	1	32
3	870.03	869.76	50	30.0	960.0	98.304	19.2	17.395	1	32
4	869.97	869.76	50	30.0	960.0	157.28 6	19.2	17.395	1	32
5	870.00	869.76	50	30.0	960.0	157.28 6	19.2	17.395	1	32
6	870.03	869.76	50	30.0	960.0	157.28 6	19.2	17.395	1	32

No.	M1	$\Delta\phi_1$	Fifa [MHz ]	Fif2 [MHz ]	Fs1 [MHz]	FD2 [KHz]	Fc2 [MHz]	K2	M2	$\Delta\phi_2$
1	5120	906	0.21	0.21	9.8304	30.000	0.21	1	328	7
2	5120	906	0.24	0.24	9.8304	30.000	0.24	1	328	8
3	5120	906	0.27	0.27	9.8304	30.000	0.27	1	328	9
4	8192	906	0.21	0.21	9.8304	30.000	0.21	1	328	7
5	8192	906	0.24	0.24	9.8304	30.000	0.24	1	328	8
6	8192	906	0.27	0.27	9.8304	30.000	0.27	1	328	9

【Table 13】

No.	Frf [MHz]	Fcp [MHz]	P	FD [KHz ]	FDP [KHz]	Fs [MHz]	FD1 [KHz]	Fc1 [MHz]	K1	L1
1	5200.0 0	5200.0 0	200	100.0	10000. 0	100.0	50.0	26.000	1	100
2	5180.0 0	5180.0 0	128	200.0	10000. 0	200.0	78.1	40.469	1	50
3	5200.0	5200.0	128	200.0	10000.	200.0	78.1	40.625	1	50

	0	0			0					
4	5220.0 0	5220.0 0	128	200.0	10000. 0	200.0	78.1	40.781	1	50

No.	M1	$\Delta\phi_1$	Fifa [MHz ]	Fif2 [MHz ]	Fs1 [MHz]	FD2 [KHz]	Fc2 [MHz]	K2	M2	$\Delta\phi_2$
1	2000	520	0.00	0.00	100	-	-	-	-	-
2	2560	518	0.00	0.00	200	-	-	-	-	-
3	2560	520	0.00	0.00	200	-	-	-	-	-
4	2560	522	0.00	0.00	200	-	-	-	-	-

5 In the receiver of the present embodiment, in the case where the frequency setting interval FDP of the quadrature demodulator 82 is settable at a step lower than or equal to the desired frequency setting interval FD of the received signal, each frequency can be input by merely changing the setting of frequency data (phase difference data) to the NCO of the local oscillator 81. Therefore, a data setting time of a controller that controls the receiver can be reduced compared with a conventional receiver and the frequency data to the NCO can be computed in a simpler manner.

10 Further, in the receiver of the present embodiment, the center frequency Fifa of the analog IF complex signal can be set to a lower value, thereby making it possible to apply a relatively small number of phase amplitude data to the local oscillator 85a using the NCO of the first embodiment, constructing the downstream frequency converter 85.

15 The NCO of the first embodiment may also be used in a transmitter as shown in Fig. 9. Fig. 9 is a block diagram illustrating the configuration of a transmitter using the NCO of the first embodiment. As illustrated in Fig. 9, the transmitter comprises a modulator 61 for modulating a carrier based on transmit data to be transmitted from the transmitter, and a roll-off filter 62 for band-limiting a complex signal (containing baseband signal components I and Q) output from the modulator 61 to a target signal band. The roll-off filter 62  
20 includes a real filter 62a and an imaginary filter 62b.

A frequency converter 63 frequency-converts an output signal from the roll-off filter 62 to obtain a complex signal of a center frequency  $F_{if2}$ . The frequency converter 63 includes a local oscillator 63a using the NCO of the first embodiment, for generating a complex local signal of a frequency  $F_{c1} = F_{if2}$  (containing a real component " $C1(t) = \cos(2\pi \times F_{c1} \times t)$ " and an imaginary component " $S1(t) = \sin(2\pi \times F_{c1} \times t)$ " whose phase is 90 degrees delayed from that of the real component), and multipliers 63b, 63c, 63d and 63e, a subtracter 63f and an adder 63g for performing multiplication, subtraction and addition operations with respect to the output signal from the roll-off filter 62 and the complex local signal generated by the local oscillator 63a, respectively.

10 An interpolation band pass filter 68 interpolates and band pass filters the complex signal from the frequency converter 63. The interpolation band pass filter 68 includes real and imaginary interpolators 64a and 64b each for multiplying a sampling frequency  $F_{s1}$  of a corresponding one of real and imaginary components of the complex signal by  $N$  to convert it into a sampling frequency  $F_{s2} = F_{s1} \times N$ . The interpolation band  
 15 pass filter 68 further includes multipliers 66a and 66b for multiplying a real component " $C2(t) = \cos(2\pi \times F_{c2} \times t)$ " and an imaginary component " $S2(t) = \sin(2\pi \times F_{c2} \times t)$ " whose phase is 90 degrees delayed from that of the real component, contained in an output signal from the NCO 70a of the first embodiment, by a filter coefficient of a low pass filter 65, respectively, and real and imaginary band pass filters 67a and 67b, a subtracter  
 20 67c and an adder 67d for performing band pass filtering, subtraction and addition operations with respect to output signals from the interpolators 64a and 64b on the basis of output signals from the multipliers 66a and 66b, respectively.

A real DAC 69a and imaginary DAC 69b cooperate to convert a digital signal of the center frequency  $F_{if2}$  from the interpolation band pass filter 68 into a complex  
 25 analog IF signal of a center frequency  $F_{ifa}$ .

A local oscillator 70 includes the NCO 70a of the first embodiment, a DAC 70b for digital/analog-converting an output signal from the NCO 70a, and a PLL circuit 70c for receiving an output signal from the DAC 70b as a reference signal. A quadrature modulator 71 frequency-converts the complex analog IF signal of the center frequency  
 30  $F_{ifa}$  from the real DAC 69a and imaginary DAC 69b to output a transmit signal (real signal) of a target center frequency  $F_{rf}$ . The quadrature modulator 71 includes multipliers 71a and 71b for multiplying real and imaginary components of the complex

analog IF signal from the real DAC 69a and imaginary DAC 69b by a real component “ $C3(t) = \cos(2\pi \times F_{cp} \times t)$ ” and an imaginary component “ $S3(t) = \sin(2\pi \times F_{cp} \times t)$ ” whose phase is 90 degrees delayed from that of the real component, contained in a complex analog local signal of a frequency  $F_{cp}$  output from the local oscillator 70, respectively,  
 5 and a subtracter 71c for subtracting output signals from the multipliers 71a and 71b from each other.

Assuming that a multiplication ratio of the PLL circuit 70c is  $P$  and an output frequency of the NCO 70a is  $F_{c2}$ , the local oscillator 70 outputs an analog local signal of a frequency  $F_{cp} = F_{rf} - F_{if} = F_{c2} \times P$ . Also, a frequency setting step  $FDP$  of the analog  
 10 local signal (frequency setting interval of the quadrature modulator 71) is a multiplication of a frequency setting step  $FD$  of the NCO 70a by  $P$ .

For example, assuming that a desired frequency setting interval  $FD$  of a transmit signal is above a frequency setting interval  $FDP$  of the quadrature modulator 71 and is indivisible by it; the transmitter is operated in the following manner. In this case, if  $K1$ ,  
 15  $K2$  and  $L2$  are arbitrary integers, the frequency converter 63 sets phase difference data  $\phi1$  to the local oscillator 63a using the NCO of the first embodiment to a value of  $\phi1 = F_{c1}/FD1 = F_{c1}/(FD \bmod FDP) \times K1$ . The frequency converter 63 converts a complex signal (containing baseband signal components  $I$  and  $Q$ ) of a sampling frequency  $F_{s1}$  output from the modulator 61 into a complex signal of a center frequency  $F_{if2}$  using a  
 20 complex local signal of a frequency  $F_{c1}$  output from the local oscillator 63a and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = (FD \bmod FDP)/K1$ . Here, the local oscillator 63a outputs the complex local signal of the frequency  $F_{c1}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M1$  as a modulus, where  $M1 = F_{s1}/(FD \bmod FDP) \times K1$ .

Also, the quadrature modulator 71 sets phase difference data  $\phi2$  to the NCO 70a of the first embodiment operating at a sampling frequency  $F_s$  to a value of  $\phi2 = F_{c2}/FDP = F_{c2}/FD \times K2/L2$ . The quadrature modulator 71 converts an analog IF signal of a center frequency  $F_{if}$ , generated by digital/analog-converting a digital IF signal of the center frequency  $F_{if2}$  by the real DAC 69a and imaginary DAC 69b, into a transmit  
 25 signal (real signal) of a target center frequency  $F_{rf}$  using an analog local signal of a frequency  $F_{cp}$  output from the local oscillator 70 and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K2 \times L2$ . The local oscillator 70 outputs the analog  
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local signal of the frequency  $F_{cp}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M2$  as a modulus, where  $M2 = F_s/FD \times K2/L2 \times P$ .

However, for example, assuming that a desired frequency setting interval  $FD$  of a transmit signal is below a frequency setting interval  $FDP$  of the quadrature modulator 71 and  $FDP$  is indivisible by  $FD$ , the frequency converter 63 sets phase difference data  $\phi1$  to the local oscillator 63a using the NCO of the first embodiment to a value of  $\phi1 = F_{c1}/FD1 = F_{c1}/(FDP \bmod FD) \times K1$ . Then, the frequency converter 63 converts a complex signal (containing baseband signal components  $I$  and  $Q$ ) of a sampling frequency  $F_{s1}$  output from the modulator 61 into a complex signal of a center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_{c1}$  output from the local oscillator 63a and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = (FDP \bmod FD)/K1$ .

Here, the local oscillator 63a outputs the complex local signal of the frequency  $F_{c1}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M1$  as a modulus, where  $M1 = F_{s1}/(FDP \bmod FD) \times K1$ .

Also, the quadrature modulator 71 sets phase difference data  $\phi2$  to the NCO 70a of the first embodiment operating at a sampling frequency  $F_s$  to a value of  $\phi2 = F_{c2}/FDP = F_{c2}/FD \times K2/L2$ . Then, the quadrature modulator 71 converts an analog IF signal of a center frequency  $F_{ifa}$ , generated by digital/analog-converting a digital IF signal of the center frequency  $F_{if2}$  by the real DAC 69a and imaginary DAC 69b, into a transmit signal (real signal) of a target center frequency  $F_{rf}$  using an analog local signal of a frequency  $F_{cp}$  output from the local oscillator 70 and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K2 \times L2$ . The local oscillator 70 outputs the analog local signal of the frequency  $F_{cp}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M2$  as a modulus, where  $M2 = F_s/FD \times K2/L2 \times P$ .

Alternatively, for example, assuming that a desired frequency setting interval  $FD$  of a transmit signal is higher than or equal to a frequency setting interval  $FDP$  of the quadrature modulator 71 and is evenly divisible by it, or that  $FD$  is lower than  $FDP$  and  $FDP$  is evenly divisible by  $FD$ , the transmitter is operated in the following manner. In this case, the frequency converter 63 sets phase difference data  $\phi1$  to the local oscillator 63a using the NCO of the first embodiment to a value of  $\phi1 = F_{c1}/FD1 = F_{c1}/FD \times K1$ . The frequency converter 63 converts a complex signal (containing baseband signal

components I and Q) of a sampling frequency  $F_{s1}$  output from the modulator 61 into a complex signal of a center frequency  $F_{if2}$  using a complex local signal of a frequency  $F_{c1}$  output from the local oscillator 63a and set to a frequency setting interval of an  $FD1$  step, where  $FD1 = FD/K1$ . Here, the local oscillator 63a outputs the complex local  
 5 signal of the frequency  $F_{c1}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M1$  as a modulus, where  $M1 = F_{s1}/FD \times K1$ .

Also, the quadrature modulator 71 sets phase difference data  $\phi2$  to the NCO 70a of the first embodiment operating at a sampling frequency  $F_s$  to a value of  $\phi2 = F_{c2}/FDP = F_{c2}/FD \times K2/L2$ . Then, the quadrature modulator 71 converts an analog IF  
 10 signal of a center frequency  $F_{ifa}$ , generated by digital/analog-converting a digital IF signal of the center frequency  $F_{if2}$  by the real DAC 69a and imaginary DAC 69b, into a transmit signal (real signal) of a target center frequency  $F_{rf}$  using an analog local signal of a frequency  $F_{cp}$  output from the local oscillator 70 and set to a frequency setting interval of an  $FDP$  step, where  $FDP = FD/K2 \times L2$ . Here, the local oscillator 70 outputs  
 15 the analog local signal of the frequency  $F_{cp}$  by accumulating the phase difference data by a modulo operation taking the nearest integer of  $M2$  as a modulus, where  $M2 = F_s/FD \times K2/L2 \times P$ .

However, in the case where a multiple of the frequency setting interval  $FDP$  of the quadrature modulator 71 is equal to that of the frequency setting interval  $FD$  of the  
 20 transmit signal, the transmitter with the above-described configuration can frequency-convert the transmit signal into the transmit signal (real signal) of the target center frequency  $F_{rf}$  by means of only the quadrature modulator 71. In this case, the frequency conversion by the frequency converter 63 may be stopped.

In the transmitter of the present embodiment, in the case where the frequency  
 25 setting interval  $FDP$  of the quadrature modulator 71 is settable at a step lower than or equal to the desired frequency setting interval  $FD$  of the transmit signal, each frequency can be output by merely changing the setting of frequency data (phase difference data) to the NCO of the local oscillator 70. Therefore, a data setting time of a controller that controls the transmitter can be reduced compared with a conventional transmitter and  
 30 the frequency data to the NCO can be computed in a simpler manner.

As described above, the NCO of the first embodiment uses the nearest integer of  $M$ , where  $M = F_s/FD \times K/L$ , on the assumption that  $F_s$  is a sampling frequency of an output signal from the NCO,  $FD$  is the upper limit of a desired frequency setting interval of the output signal and  $K$  and  $L$  are arbitrary integers. The phase calculator 1b  
 5 generates phase data by performing a modulo operation taking the integral  $M$  as a modulus with respect to input phase difference data and phase data from the phase register 1a. The ROM 2 stores a phase/amplitude conversion table including  $M$  amplitude data and outputs amplitude data corresponding to the generated phase data through its data terminal. Therefore, it is possible to realize a low-spurious NCO which  
 10 provides its output signal set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ .

Therefore, because a low-spurious NCO, which provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval is realized on the basis of only low-capacity, amplitude data of  $M$  number that is smaller  
 15 than a conventional one, it can be reduced in power consumption and cost.

Further, it is possible to realize the digital down-converter, the digital up-converter, the receiver with the demodulator, and the transmitter with the modulator of the second to eighth embodiments using the NCO of the first embodiment. As a result, the digital down-converter, digital up-converter, receiver, or transmitter can be reduced  
 20 in power consumption and cost compared with a conventional one.

As apparent from the above description, if the upper limit of a desired frequency setting interval of an output signal is  $FD$ , and  $K$  and  $L$  are arbitrary integers, a phase accumulator generates phase data by accumulating input phase difference data by a modulo operation taking the nearest integer of  $M$  as a modulus, where  $M = F_s/FD \times K/L$ ,  
 25 and outputs the generated phase data as an address input to a phase/amplitude conversion table. As a result, the phase/amplitude conversion table outputs amplitude data corresponding to the input phase data as an output signal of the NCO set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ .

Therefore, a low-spurious NCO, which provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval, can  
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be realized on the basis of only low-capacity, amplitude data of M number that is smaller than a conventional one, so it can be reduced in power consumption and cost.

According to a digital down-converter of the present invention, a frequency converter frequency-converts an input signal using a frequency signal output from the NCO of claim 1 as a local oscillator and set to a frequency setting interval of a  $dF$  step, where  $dF = FD/K \times L$ . In the case where a desired frequency setting interval  $FD$  of the input signal is higher than or equal to a frequency setting interval  $dF$  of the frequency converter and is evenly divisible by it, the digital down-converter can convert the frequency of the input signal input thereto at the frequency setting interval  $FD$  into a desired frequency within the range of an allowable frequency deviation.

Therefore, the use of the low-spurious NCO which is realized on the basis of only low-capacity, amplitude data of M number that is smaller than a conventional one, where  $M = Fs/FD \times K/L$ , and provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval can reduce power consumption and cost of the digital down-converter that can convert the frequency of the input signal input thereto at the desired frequency setting interval into a desired frequency within the range of an allowable frequency deviation.

According to an alternative digital down-converter of the present invention, one of two frequency converters provided for frequency conversions includes a low-spurious NCO which is realized on the basis of only  $M1$  low-capacity amplitude data and provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval, and the other includes a low-spurious NCO which is realized on the basis of only  $M2$  low-capacity amplitude data and provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval. The digital down-converter is able to cope with the case where a frequency setting interval  $FD$  of an input signal is above a frequency setting interval  $FD1$  of the first frequency converter and is indivisible by it, the case where the frequency setting interval  $FD$  is below the frequency setting interval  $FD1$  and  $FD1$  is indivisible by  $FD$ , and the case where the frequency setting interval  $FD$  is higher than or equal to the frequency setting interval  $FD1$  and is evenly divisible by it, or  $FD$  is lower than  $FD1$  and  $FD1$  is evenly divisible by  $FD$ , respectively.

Therefore, the use of the two low-spurious NCOs which are realized on the basis of only low-capacity, amplitude data of M1 and M2 numbers that are each smaller than a conventional one and provide their output signals each set to a frequency setting interval lower than or equal to a desired frequency setting interval can reduce power  
 5 consumption and cost of the digital down-converter that can convert the frequency of the input signal input thereto at the desired frequency setting interval into a desired frequency within the range of an allowable frequency deviation.

According to yet another digital down-converter of the present invention, in the case where a multiple of the frequency setting interval FD1 of the first frequency  
 10 converter is equal to that of the frequency setting interval FD of the input signal, the digital down-converter can convert the frequency of the input signal input thereto at the frequency setting interval FD into a desired frequency within the range of an allowable frequency deviation by means of only the first frequency converter.

Therefore, it is possible to reduce power consumption of the digital  
 15 down-converter that can convert the frequency of the input signal input thereto at the desired frequency setting interval into a desired frequency within the range of an allowable frequency deviation.

According to another embodiment of a digital up-converter of the present invention, a frequency converter frequency-converts an input signal using a frequency  
 20 signal output from the NCO of claim 1 as a local oscillator and set to a frequency setting interval of a dF step, where  $dF = FD/K \times L$ . In the case where a desired frequency setting interval FD of an output signal is higher than or equal to a frequency setting interval dF of the frequency converter and is evenly divisible by it, the digital up-converter can set the frequency setting interval of its output signal to FD.

Therefore, the use of the low-spurious NCO which is realized on the basis of only low-capacity, amplitude data of M number that is smaller than a conventional one, where  $M = F_s/FD \times K/L$ , and provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval can reduce power  
 25 consumption and cost of the digital up-converter that can output a signal of the desired frequency setting interval.  
 30

According to alternative digital up-converters of the present invention, one of two frequency converters provided for frequency conversions includes a low-spurious NCO which is realized on the basis of only M1 low-capacity amplitude data and provides its output signal set to a frequency setting interval lower than or equal to a  
5 desired frequency setting interval, and the other includes a low-spurious NCO which is realized on the basis of only M2 low-capacity amplitude data and provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval. The digital up-converter is able to cope with the case where a frequency setting interval FD of an output signal is above a frequency setting interval FD2 of the  
10 second frequency converter and is indivisible by it, the case where the frequency setting interval FD is below the frequency setting interval FD2 and FD2 is indivisible by FD, and the case where the frequency setting interval FD is higher than or equal to the frequency setting interval FD2 and is evenly divisible by it, or FD is lower than FD2 and FD2 is evenly divisible by FD, respectively.

15 Therefore, the use of the two low-spurious NCOs which are realized on the basis of only low-capacity, amplitude data of M1 and M2 numbers that are each smaller than a conventional one and provide their output signals each set to a frequency setting interval lower than or equal to a desired frequency setting interval can reduce power consumption and cost of the digital up-converter that can output a signal of the desired  
20 frequency setting interval.

According to a digital up-converter of the present invention, in the case where a multiple of the frequency setting interval FD2 of the second frequency converter is equal to that of the frequency setting interval FD of the output signal, the digital up-converter can set the frequency setting interval of its output signal to FD by means of only the  
25 second frequency converter.

Therefore, it is possible to reduce power consumption of the digital up-converter that can output a signal of the desired frequency setting interval.

According to the preferred embodiments of the receiver of the present invention, one of two frequency converters provided for frequency conversion of a received signal  
30 into an input signal desired by a demodulator includes a low-spurious NCO which is realized on the basis of only M1 low-capacity amplitude data and provides its output

signal set to a frequency setting interval lower than or equal to a desired frequency setting interval, and the other includes a low-spurious NCO which is realized on the basis of only M2 low-capacity amplitude data and provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval.

- 5 The receiver is able to cope with the case where a frequency setting interval FD of an input signal is above a frequency setting interval FDP of the first frequency converter and is indivisible by it, the case where the frequency setting interval FD is below the frequency setting interval FDP and FDP is indivisible by FD, and the case where the frequency setting interval FD is higher than or equal to the frequency setting interval FDP and is evenly divisible by it, or FD is lower than FDP and FDP is evenly divisible by FD, respectively.
- 10

Therefore, the use of the two low-spurious NCOs which are realized on the basis of only low-capacity, amplitude data of M1 and M2 numbers that are each smaller than a conventional one and provide their output signals each set to a frequency setting interval lower than or equal to a desired frequency setting interval can reduce power consumption and cost of the receiver that can accurately convert the frequency of the received signal input thereto at the frequency setting interval FD into that desired by the demodulator.

15

According to an alternate embodiment of the receiver of the present invention, in the case where a multiple of the frequency setting interval FD1 of the first frequency converter is equal to that of the frequency setting interval FD of the received signal, the receiver can accurately convert the frequency of the received signal input thereto at the frequency setting interval FD into that desired by the demodulator by means of only the first frequency converter.

20

Therefore, it is possible to reduce power consumption of the receiver that can accurately convert the frequency of the received signal input thereto at the frequency setting interval FD into that desired by the demodulator.

25

According to preferred embodiments of a transmitter of the present invention, one of two frequency converters provided for frequency conversion of a transmit signal from a modulator into a target frequency includes a low-spurious NCO which is realized on the basis of only M1 low-capacity amplitude data and provides its output signal set to

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a frequency setting interval lower than or equal to a desired frequency setting interval, and the other includes a low-spurious NCO which is realized on the basis of only M2 low-capacity amplitude data and provides its output signal set to a frequency setting interval lower than or equal to a desired frequency setting interval. The transmitter is  
5 able to cope with the case where a frequency setting interval FD of an output signal is above a frequency setting interval FDP of the second frequency converter and is indivisible by it, the case where the frequency setting interval FD is below the frequency setting interval FDP and FDP is indivisible by FD, and the case where the frequency setting interval FD is higher than or equal to the frequency setting interval FDP and is  
10 evenly divisible by it, or FD is lower than FDP and FDP is evenly divisible by FD, respectively.

Therefore, the use of the two low-spurious NCOs which are realized on the basis of only low-capacity, amplitude data of M1 and M2 numbers that are each smaller than a conventional one and provide their output signals each set to a frequency setting interval  
15 lower than or equal to a desired frequency setting interval can reduce power consumption and cost of the transmitter that can accurately convert the frequency of the baseband transmit signal from the modulator into a target transmit signal frequency.

According to an alternative embodiment transmitter of the present invention, in the case where a multiple of the frequency setting interval FD2 of the second frequency  
20 converter is equal to that of the frequency setting interval FD of the transmit signal, the transmitter can accurately convert the frequency of the baseband transmit signal from the modulator into that of a target transmit signal by means of only the second frequency converter.

Therefore, it is possible to reduce power consumption of the transmitter that can  
25 accurately convert the frequency of the baseband transmit signal from the modulator into a target transmit signal frequency.

Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope  
30 and spirit of the invention as disclosed in the accompanying claims.